(2)

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

ON THE DESIGN AND ANALYSIS OF
MULTIPLE-STORAGE ELEMENTS

by

David A. York

December 1989

Thesis Advisor: Jon T. Butler

Approved for public release; distribution is unlimited

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No 0704-0188

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution is unlimited
2b DECLASSIFICATION / DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S)
6a NAME OF PERFORMING ORGANIZATION Naval Postgraduate School 6b OFFICE SYMBOL (If applicable) 62	7a NAME OF MONITORING ORGANIZATION Naval Postgraduate School
6c ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000	7b ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000
8a NAME OF FUNDING / SPONSORING ORGANIZATION 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c ADDRESS (City, State, and ZIP Code)	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO / PROJECT NO / TASK NO / WORK UNIT ACCESSION NO
11 TITLE (Include Security Classification) ON THE DESIGN AND ANALYSIS OF MULTIPLE-VALUED STORAGE ELEMENTS	
12 PERSONAL AUTHOR(S) YORK, David A.	
13a TYPE OF REPORT Master's Thesis 13b TIME COVERED FROM _____ TO _____	14 DATE OF REPORT (Year, Month, Day) 1989 December 15 PAGE COUNT 107
16 SUPPLEMENTARY NOTATION The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the US Government.	
17 COSATI CODES FIELD / GROUP / SUB-GROUP	18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number) data latch; memory element; flip-flop; CMOS logic circuits; clocked storage device; multiple-valued logic

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

The primary contribution of this thesis is the development of a data storage latch that accepts, stores and provides four-valued logic signals. The latch is implemented in ~~CMOS~~ and all logic levels are encoded as voltage. The latch storage state is determined by thresholding operations on its input, and the output is logically restored replica of that (multiple-valued) input. Detailed analysis of an existing current-mode CMOS design is also presented in this study. A comparison between these devices reveals that the voltage-mode data latch provides less stable intermediate logic states, but consumes significantly less static power. In addition, the voltage-mode CMOS design can be implemented with the same number of devices that are required for two binary "D" flip-flops.

20 DISTRIBUTION / AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL BUTLER, Jon T.	22b TELEPHONE (Include Area Code) 408-646-3299 22c OFFICE SYMBOL 62Bu

DD Form 1473, JUN 86 *Previous editions are obsolete*

S/N 0102-LF-014-6603

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

Approved for public release; distribution is unlimited

On the Design and Analysis of Multiple-Valued Storage Elements

by

David A. York
Lieutenant, United States Navy
B.S., University of Missouri, 1981

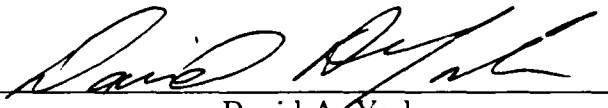
Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

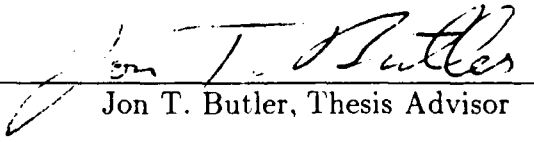
from the

NAVAL POSTGRADUATE SCHOOL

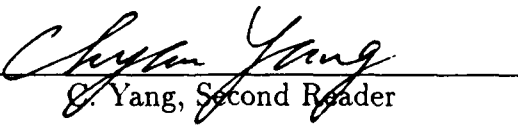
December 1989

Author: 

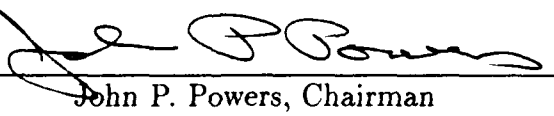
David A. York

Approved by: 

Jon T. Butler, Thesis Advisor



C. Yang, Second Reader



John P. Powers, Chairman
Department of Electrical and Computer Engineering

ABSTRACT

The primary contribution of this thesis is the development of a data storage latch that accepts, stores and provides four-valued logic signals. The latch is implemented in CMOS and all logic levels are encoded as voltage. The latch storage state is determined by thresholding operations on its input, and the output is a logically restored replica of that (multiple-valued) input. Detailed analysis of an existing current-mode CMOS design is also presented in this study. A comparison between these devices reveals that the voltage-mode data latch provides less stable intermediate logic states, but consumes significantly less static power. In addition, the voltage-mode CMOS design can be implemented with the same number of devices that are required for two binary "D" flip-flops.

TABLE OF CONTENTS

I. INTRODUCTION 1

A. POTENTIAL BENEFITS OF MVL 1

B. APPLICATIONS OF MVL 2

C. PROBLEMS WITH MVL 3

II. THEORETICAL BACKGROUND 6

A. SYMBOLS AND ABBREVIATIONS 6

B. MOS DEVICE CHARACTERISTICS 7

C. THE CURRENT-MODE CMOS CONCEPT 9

1. Diode-Connected Transistors 9

2. Current Mirrors 10

3. Current-Controlled Inverter 12

4. *Current Comparator* 14

5. Current Encoder 16

III. AN EXISTING CURRENT-MODE CMOS DESIGN 18

A. OVERALL OPERATION 18

B. SELECTION OF THE REFERENCE VOLTAGE 20

C. THE COMPARATOR SUBCIRCUIT 24

D. THE ENCODER SUBCIRCUIT 28

E. FORMING THE OUTPUT 34

F. OVERALL CIRCUIT SIMULATIONS 36

IV. MODIFIED CURRENT-MODE CMOS DESIGN 44

A. CURRENT CONTROLLED INVERTERS 44

B. DIRECT USE OF THE COMPARATOR OUTPUT VOLTAGES . 46

V. VOLTAGE-MODE CMOS DESIGNS 51
A. INPUT THRESHOLDING 51
B. VOLTAGE ENCODER 53
C. A 15 V CMOS DATA LATCH DESIGN 54
D. A 5 VOLT CMOS DATA LATCH 61
E. INTERMEDIATE VOLTAGE GENERATION 66
VI. COMPARISONS BETWEEN DESIGNS 72
A. STATIC POWER REQUIREMENTS 72
B. SPEED 74
C. CIRCUIT COMPLEXITY 75
VII. MVL VS. BINARY 77
VIII. CONCLUSIONS 81
APPENDIX A: PSPICE MODEL PARAMETERS 83
APPENDIX B: PSPICE INPUT DATA FILES 85
REFERENCES 93
INITIAL DISTRIBUTION LIST 95

LIST OF TABLES

2.1 CURRENT ENCODER I/O CHARACTERISTICS 17

3.1 COMPARATOR RESPONSE TO CURRENT INPUTS 19

3.2 COMPARATOR CURRENT SOURCE TRANSISTOR GEOMETRIES 25

5.1 THRESHOLD DETECTOR RESPONSE 53

5.2 ENCODER RESPONSE TO LOGICAL INPUTS 55

5.3 COMPARISON OF VOLTAGE-MODE DELAY TIMES 66

6.1 STATIC POWER CONSUMPTION 74

7.1 MVL VS BINARY - CIRCUIT COMPLEXITY 78

LIST OF FIGURES

2.1 CMOS Transistors 7

2.2 Diode-Connected Transistors 10

2.3 CMOS Current Mirror 11

2.4 Current-Controlled CMOS Inverter 13

2.5 CMOS Current Comparator (After Ref. 13) 14

2.6 Three State CMOS Current Encoder (After Ref. 13) 17

3.1 Four-Valued Current-Code CMOS Data Latch (After Ref. 13) 18

3.2 Reference Voltage Generator (After Ref. 13) 20

3.3 Comparator Leg I-V Characteristics 22

3.4 The Comparator Subcircuit (After Ref. 13) 24

3.5 Comparator Leg Response to a Ramped Input Current 27

3.6 Comparator Output Control Signals V_A, V_B, V_C 28

3.7 The Encoder Subcircuit (After Ref. 13) 29

3.8 An Encoder Test Circuit 30

3.9 Encoder Test Circuit Output 31

3.10 Individual Contributions to Encoder Output Current Spikes 32

3.11 Parasitic Capacitance in a MOSFET Transistor 33

3.12 The Output Subcircuit (After Ref. 13) 34

3.13 Four-Valued Current-Mode CMOS Data Latch (From Ref. 13) 36

3.14 Circuit Response in the Setup Mode 38

3.15 Latch Output in the Hold Mode 39

3.16 Latch Response to Step Inputs 40

3.17 Vgs Developed Across Transistor M_1 (Step Up Inputs) 41

3.18 Vgs Developed Across Transistor M_7 (Step Down Inputs) 42
3.19 Clocked Operations 43
4.1 Modified Latch Using Current Controlled Inverters 44
4.2 Vgs_1 as a Function of Iin 45
4.3 Modified Current-Mode CMOS Four-Valued Data Latch 47
4.4 Modified Latch I/O Characteristics 48
4.5 Comparison of Latch I/O Characteristics 49
4.6 Modified Latch Response to Step Inputs 50
5.1 CMOS Inverters as Threshold Detectors 52
5.2 Standard CMOS Inverter 53
5.3 Voltage Encoder 54
5.4 CMOS Realization of a Four-Valued Voltage Encoder 55
5.5 Four-Valued Voltage-Mode CMOS Data Latch 56
5.6 Threshold Detector DC Characteristics (Vdd = 15 V) 57
5.7 Latch Input/Output DC Characteristics (Vdd = 15 V) 58
5.8 Latch Response to Step Inputs (Vdd = 15 V) 59
5.9 Clocked Operations (Vdd = 15 V) 60
5.10 Latch Output as a Function of V_{logic1} 62
5.11 Threshold Detector DC Characteristics (Vdd = 5 V) 63
5.12 Latch Input/Output DC Characteristics (Vdd = 5 V) 64
5.13 Latch Response to Step Inputs (Vdd = 5 V) 65
5.14 Clocked Operations (Vdd = 5 V) 67
5.15 Voltage-Divider Network 68
5.16 Modified Voltage-Mode Four-Valued Data Latch 69
5.17 Modified Latch Input/Output DC Characteristics 69
5.18 Modified Latch Response to Step Inputs 70

5.19 Modified Latch Clocked Operations 71

7.1 Binary Data Latch 78

7.2 Four-State Latch Using Binary Devices 79

ACKNOWLEDGMENT

I would like to express my gratitude and appreciation to the faculty and staff of the Electrical and Computer Engineering department for providing me with the opportunity and encouragement to explore many exciting facets of electrical engineering. I would like to offer special thanks to Professors J. Butler and C. Yang for their patience and unselfish assistance, and to Professor M. Cotton for hours of his valuable time concerning VLSI, Magic and SPICE.

Mostly, I wish to thank my wife, Robin, and two daughters, Cary and Mandy. Their patience and support for the duration of this project was both appreciated and much needed.

I. INTRODUCTION

A. POTENTIAL BENEFITS OF MVL

CMOS memories exceeded one million devices in 1987, with up to 100 million expected by 1995 [Ref. 1]. Achieving this goal will require innovative design techniques, since severe physical limitations are rapidly being approached. Inter-device connections currently require more chip area than the active logic elements themselves. With estimates of up to 70 percent of the VLSI chip area being devoted to those connections, this limitation may prove difficult to overcome by present methods [Ref. 2]. In addition to inter-device connections, the number of input/output (I/O) pins capable of being placed within a chip package has also become a significant binary design problem. Although IC manufacturers are successfully exploiting the concept of time-multiplexing [Ref. 1], multiple-valued logic (MVL) could become an attractive option for future chip designs.

Through the use of MVL, more information can be carried by connections. For example, converting a connection from 2-valued to 4-valued doubles its information capability [Ref. 2]. The importance of multiple-valued logic is that "information", rather than "devices", can be packed into a chip or onto a wire. With more information carried per line, the interconnection requirements between devices can be reduced and the information available per I/O pin is increased.

MVL can also increase circuit functionality. With a single binary variable, only four output functions can be performed: identity function (output is the same as the input), complement of the input, constant 0, or constant 1. However, if the variable is four-valued, there are $4^4 = 256$ possible input/output relationships [Ref. 3].

Therefore, MVL not only increases the amount of information available per line (variable), but increases the ability to manipulate that information as well.

B. APPLICATIONS OF MVL

The potential benefits of MVL have not gone unnoticed by commercial IC manufacturers. In 1978, the first four-valued memory was developed by M. Yamaha in Japan; the first four-valued implementations of logic operations were developed in 1979 [Ref. 4]; and, in 1980, Intel's 8087 numeric coprocessor and the iAXP-432 microprocessor used four-valued ROM in their construction [Refs. 2, 3]. Motorola and General Instrument have even used a four-valued ROM in the development of an electronic toy's speech synthesizer [Ref. 3].

The use of MVL has resulted in improvements in both chip area and device speed. Intel's use of a four-valued NMOS ROM in their 8087 arithmetic coprocessor resulted in a 31 percent reduction of chip size, and Motorola's CMOS version resulted in a 30 percent reduction [Ref. 1]. Other applications include four-valued CCD memory designs by IBM and Mitsubishi, with Hitachi conducting a pre-commercial study of a 16-valued RAM prototype [Ref. 3]. For MVL logic implementations, the authors of Ref. 5 describe the design of a signed-digit, four-valued parallel adder. Its speed is independent of word length and is significantly faster than conventional binary adders. Also in Ref. 5, a multiplier was described that performs 32-bit two's complement multiplication using three stages of these radix-4 adders. Requiring only 52 percent of its binary counterpart's transistors, it occupies half the chip space, and consumes half the power. This is accomplished at a speed that is nearly identical to that of the fastest binary multiplier available. In Ref. 6, a Totally Self-Checking (TSC) circuit was designed that needs no separate error code storage. It uses three-valued logic components that have normal outputs corresponding to the fault-free circuit and its

use resulted in a reduction (by two) of the number of signal lines required for fault analysis. In recent literature [Refs. 7, 8, 9], additional components such as analog-to-digital and multiple-valued-to-binary converters, using technologies ranging from bipolar to switched capacitor networks, are also starting to appear. Though examples of actual implementation are still scarce, chip size reduction, increased information capacity and error detection are emerging as benefits from these new designs.

C. PROBLEMS WITH MVL

With the potential benefits MVL appears to provide, what has prevented MVL from revolutionizing the IC circuit industry? Although steps in this direction could be claimed to have already occurred, many problems need to be solved before MVL becomes overwhelmingly accepted as an alternative to binary.

One of these problems is speed. For example, although Motorola's ROM achieved 256 kilobytes of information at a 30 percent reduction in area, it is only capable of delivering that information at an average access time of 200 ns [Ref. 1]. Similarly, General Instrument's 40 and 128 kilobyte versions operate between 500 and 800 ns respectively. For memories of this size, typical binary access times are on the order of 30–100ns [Ref. 10]. As can be seen, significant improvements must be made in order to deliver equivalent speed.

Although increased functionality was stated as one of the major benefits MVL can provide, this is easily offset by an unavoidable increase in complexity. In a previous example, up to 256 possible input/output relationships were shown to be realizable with a single four-valued variable. Although definitely providing flexibility, just the number of functions can become completely unmanageable, especially when higher radix systems are considered. The consequence is that the usual binary practice of naming the few available functions is no longer helpful, and if a tabular format

is used, the size of the table becomes limiting as well, (the truth table for a two-variable four-valued function already requires 16 rows) [Ref. 3]. Even the notation used to describe MVL functions can become a severe problem. Though there are a few "generally" accepted methods of representing MVL functions [Refs. 3, 11, 12], there are no definitive standards. Therefore, binary functions (and methods for representing them) no longer serve the designer's needs, and an entirely different, more general approach must be used.

PLA minimization provides an excellent example of the problem. Requiring only a small subset of an otherwise fully addressable ROM, PLA's have become extremely popular in the design of digital systems. To make the PLA useful, however, designers must meet functionality requirements within some minimal set of required operations. The function to be implemented must therefore be reduced, in an algebraic sense, before it is known whether a PLA will be be beneficial to the design. However, the problem of finding that minimal solution, even in binary, is known to be NP-complete [Ref. 4]. Therefore, PLA minimization will be even further complicated by the more generalized approach of MVL. As a result, there are only four practical MVL PLA minimization routines known to exist, none of which guarantee minimal solutions.

The lack of system level design tools is another significant problem area. To "streamline" the system level design process, binary designers found it necessary to abandon traditional gate-level design techniques. With a hierarchy of binary building blocks already available, the transition to a functional block design concept was easily made. As a result, computer-aided-design (CAD) tools became readily available, as well as heavily used. Due to the complexity inherent in MVL, "brute force" methods (such as Karnaugh-map minimization) become extremely difficult, if not impossible to perform. Therefore, the CAD tool becomes an almost absolute necessity for the design of even the most basic MVL system. However, there are only three known to

exist, all of which deal solely with PLA minimization. In order for MVL designs to progress, the capability of these tools must be greatly expanded.

As a final observation, there are currently no known radix-4 or higher MVL sequential storage devices available. Although several designs have appeared in recent literature [Refs. 6, 13, 14], none are known to have been successfully tested. Without reliable sequential logic devices, MVL applications will continually be forced to convert intermediate component results to binary. This alone has the potential of negating many of the benefits that MVL can provide.

In summary, multiple-valued logic has the potential of providing many advantages to a digital world that is rapidly becoming hindered by physical limitations. However, many problems must be solved before extensive use of MVL becomes practical. With the lack of the most fundamental building block needed in the construction of an MVL "system", and the lack of the necessary tools required to design it, motivation for the topic of this thesis becomes apparent.

II. THEORETICAL BACKGROUND

A. SYMBOLS AND ABBREVIATIONS

This section is provided as a reference for symbols, abbreviations and frequently used constants. They will apply throughout:

CMOS	Complimentary Metal Oxide Silicon device technology
NMOS	N-type Metal Oxide Silicon Transistor
PMOS	P-type Metal Oxide Silicon Transistor
Vgs_i	Gate to source voltage for the i^{th} device
Vds_i	Drain to source voltage for the i^{th} device
Vt_n	Threshold voltage for an NMOS transistor
Vt_p	Threshold voltage for a PMOS transistor
V_{ref}	Reference voltage
V_{in}	Input voltage
V_{out}	Output voltage
V_{dd}	Circuit supply voltage
V_{sw}	Switching voltage
Gnd	Ground potential
I_{in}	Input current
I_r	Reflected current
I_{out}	Output current
Ids_i	Drain to source current for the i_{th} device
I_{sw}	Switching current
I_{th}	Threshold current

β	MOS transistor gain factor
μ	Surface mobility of electrons in the channel
ϵ	Permittivity of the gate insulator
t_{ox}	Thickness of the gate insulator
L	Transistor channel length
W	Transistor channel width
M_i	The i^{th} MOS transistor of the circuit

Before specific designs can be presented, characteristics of the components that will be used to construct them must first be considered.

B. MOS DEVICE CHARACTERISTICS

CMOS technology provides two types of metal oxide silicon (MOS) transistors on the same substrate. With Fig. 2.1 defining the current flow and voltage polarity conventions that will be used for each device, ideal behavior in three distinct regions of operation can be described as follows:

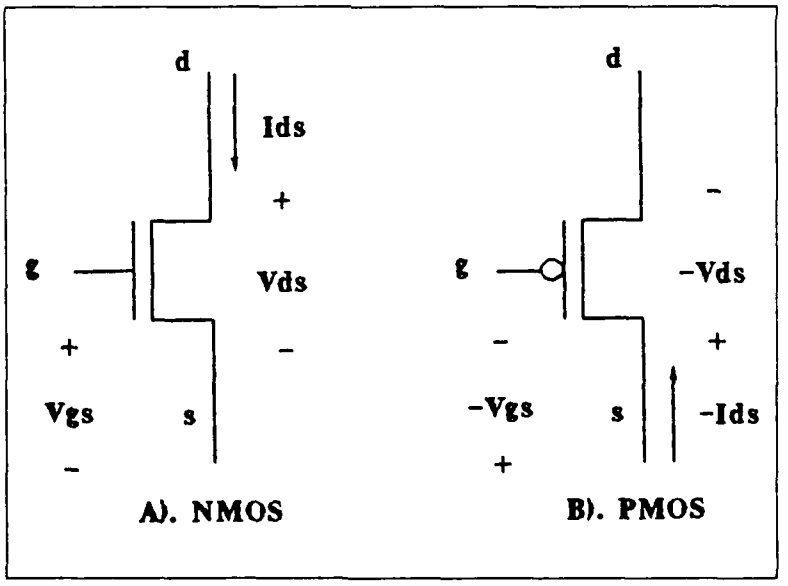


Figure 2.1: CMOS Transistors

— Cutoff: in this region, the applied gate to source voltage (Vgs) is insufficient to overcome the threshold voltage (Vt) of the device. A channel between the transistor source and drain cannot be formed and current is prevented from flowing through device.

$$for \mid Vgs - Vt \mid \leq 0 \tag{2.1}$$

$$NMOS : Ids = 0 \tag{2.2}$$

$$PMOS : -Ids = 0 \tag{2.3}$$

— Linear: this region is characterized by the presence of an induced channel between the source and drain of the transistor. A path for current flow is provided by that channel and device behavior is similar to that of a voltage controlled resistance.

$$for \;\; 0 < \mid Vds \mid < \mid Vgs - Vt \mid \tag{2.4}$$

$$NMOS : Ids = \beta[(Vgs - Vt_n)Vds - \frac{Vds^2}{2}] \tag{2.5}$$

$$PMOS : -Ids = \beta[(-Vgs + Vt_p)(-Vds) - \frac{(-Vds)^2}{2}] \tag{2.6}$$

— Saturation: in this region, Ids is independent of Vds (or nearly so).

$$for \;\; 0 < \mid Vgs - Vt \mid < \mid Vds \mid \tag{2.7}$$

$$NMOS : Ids = \frac{\beta}{2}(Vgs - Vt_n)^2 \tag{2.8}$$

$$PMOS : -Ids = \frac{\beta}{2}(-Vgs + Vt_p)^2 \tag{2.9}$$

The transistor gain factor β is an important quantity in the operation of MOS transistors. It is dependent on both process parameters and device geometry and is given by

$$\beta = \frac{\mu\epsilon}{t_{ox}}(W/L). \tag{2.10}$$

With μ ,ϵ and t_{ox} accounting for such process dependent factors as doping density and gate oxide thickness, the desired gain can be achieved by simply altering the width to length ratio (W/L) of the device. As will be shown in the sections that follow, many of the circuit characteristics needed for MVL applications are obtained through the use of this parameter alone.

C. THE CURRENT-MODE CMOS CONCEPT

The most commonly-used quantity for CMOS logic level encryption is voltage. However, CMOS implementations of MVL storage devices need not be restricted to the use of voltage-encoded logic signals. Current may also be used. Since the operation of current-mode CMOS components significantly differ from those of standard CMOS designs, this section has been included to provide a basic understanding of those devices.

1. Diode-Connected Transistors

A fundamental component used in current-mode CMOS designs is the diode-connected transistor. With both n and p device types shown in Fig. 2.2, diode-connected transistors allow current to flow in only one direction.

For the n device, since the gate and drain are physically connected,

$$Vgs - Vt_n = Vds - Vt_n. \tag{2.11}$$

With $Vt_n > 0$,

$$Vds - Vt_n < Vds, \tag{2.12}$$

and therefore,

$$Vgs - Vt_n < Vds. \tag{2.13}$$

Operation outside cutoff requires $Vgs - Vt_n > 0$, and with $Vgs = Vds$, we obtain

$$0 < Vgs - Vt_n < Vds, \quad for \quad Vds > Vt_n. \tag{2.14}$$

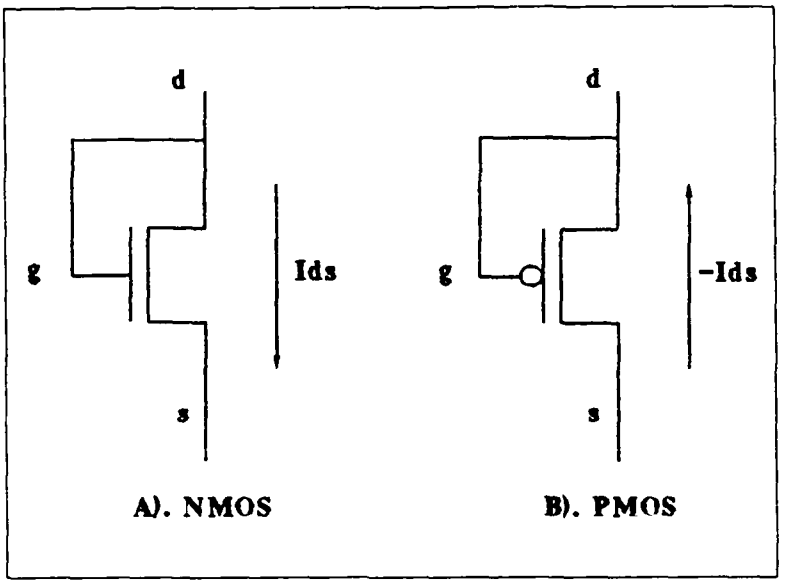


Figure 2.2: Diode-Connected Transistors

Provided $Vgs > Vt_n$, Equation 2.14 corresponds to saturation, in which case Ids_n is given by

$$Ids_n = \frac{\beta_n}{2}(Vgs - Vt_n)^2. \tag{2.15}$$

However, if Vds falls below the transistor threshold voltage, the diode-connected transistor will operate in cutoff and $Ids_n = 0$. As a result, current is only allowed to flow in one direction.

P-type device equations may be obtained by reversing the polarity of Vt, Vds, Vgs and Ids in Equations 2.11 through 2.15 above. Performing these substitutions will yield:

$$-Ids_p = \frac{\beta_p}{2}(-Vgs + Vt_p)^2, \quad for \mid -Vgs \mid > \mid Vt_p \mid . \tag{2.16}$$

2. Current Mirrors

Another component fundamental to current-mode CMOS designs is the current mirror. With one example shown in Fig. 2.3, current mirrors provide one of the few means available for replicating current-encoded signals.

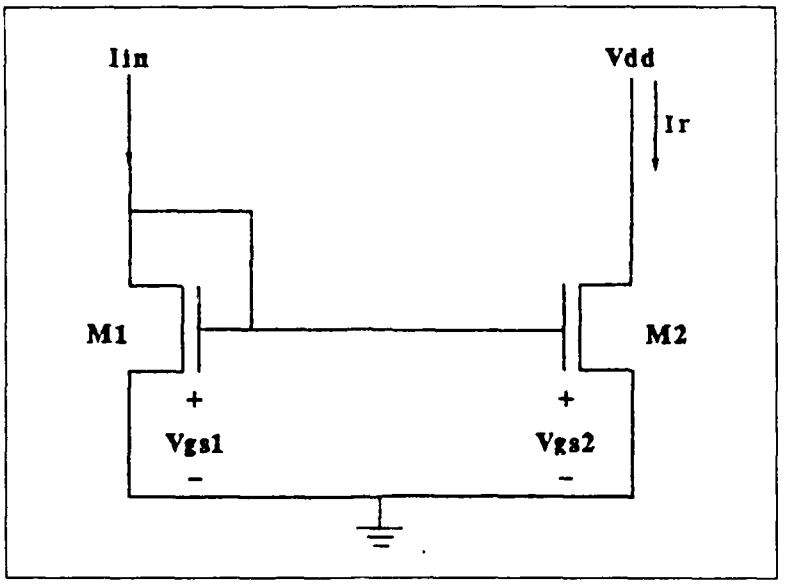


Figure 2.3: CMOS Current Mirror

In Fig. 2.3, an external input current, (I_{in}) is applied to the drain of transistor M_1. Since M_1 is diode connected, the current $Ids_1 = I_{in}$ will pass through M_1 to ground and a voltage (Vgs_1) will be induced across the device. Equation 2.15 can be rearranged to obtain

$$Vgs_1 = \sqrt{\frac{2I_{in}}{\beta_1}} + Vt_n, \quad for \quad I_{in} \geq 0, \tag{2.17}$$

and, with transistors M_1 and M_2 sharing a common gate,

$$Vgs_2 = Vgs_1. \tag{2.18}$$

Assuming I_{in} is limited such that

$$max\{Vgs_2\} \leq V_{dd}, \tag{2.19}$$

then

$$Vgs_2 - Vt_n < Vds_2, \tag{2.20}$$

which forces transistor M_2 to operate in saturation. From Equation 2.8, the current

through M_2 can be described by

$$Ids_2 = \frac{\beta_2}{2}(Vgs_2 - Vt_n)^2 = I_r, \tag{2.21}$$

and with $Vgs_2 = Vgs_1$,

$$I_r = \frac{\beta_2}{2}[(\sqrt{\frac{2I_{in}}{\beta_1}} + Vt_n) - Vt_n]^2 = \frac{\beta_2}{\beta_1}I_{in}, \quad for \quad I_{in} \geq 0. \tag{2.22}$$

With process dependent factors μ, ϵ and t_{ox} assumed constant, substituting Equation 2.10 for β_1 and β_2 yields

$$I_r = \left(\frac{W_2/L_2}{W_1/L_1}\right) I_{in}, \quad for \quad I_{in} \geq 0. \tag{2.23}$$

Therefore, the current mirror provides a multiple of its input as the circuit output. For equivalent width to length ratios, the output becomes a replica of the input current.

3. Current-Controlled Inverter

With the addition of a PMOS transistor, as shown in Fig. 2.4, the current mirror can be made to perform the function of a current-controlled voltage inverter.

With $I_{in} = 0$, no gate-to-source voltage is induced across transistors M_1 or M_2. Under these conditions, M_2 is in cutoff and no path from node A to ground exists. Since

$$| Vgs_3 - Vt_p | > | Vds_3 |, \tag{2.24}$$

M_3 will operate in the linear region, and as a result,

$$V_{out} = V_{dd}. \tag{2.25}$$

When a small input current is applied, the gate voltages of M_1, M_2 and M_3 will rise; M_2 will bias on in saturation (as in the current mirror application); and, as I_{in} is increased, V_{out} will drop in value. With

$$| Vds_3 | = | V_{out} - V_{dd} |, \tag{2.26}$$

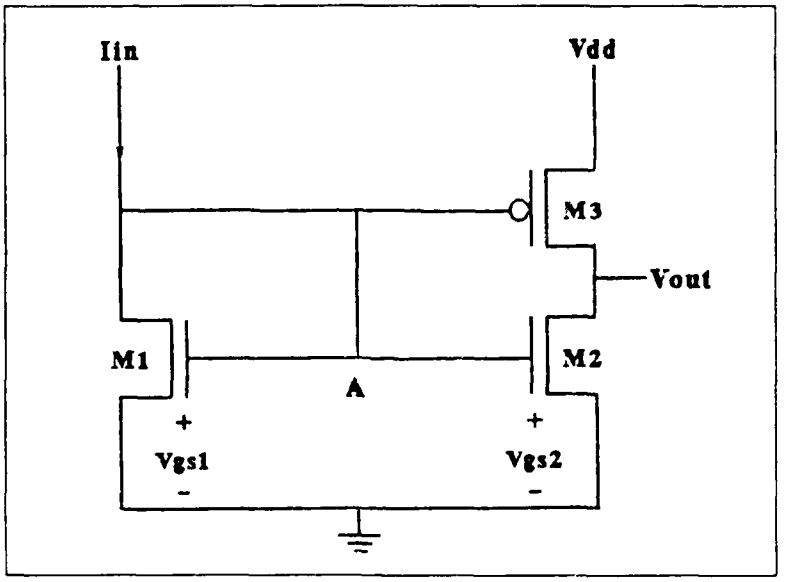


Figure 2.4: Current-Controlled CMOS Inverter

a point will be reached where both M_2 and M_3 operate in saturation and the logical state of V_{out} will transition from high to low. The input voltage (Vgs_1) at which this occurs is defined as the inverter switching voltage (V_{sw}), and can be obtained as follows: From Equations 2.8 and 2.9,

$$Ids_2 = \frac{\beta_2}{2}(Vgs_2 - Vt_n)^2 = \frac{\beta_2}{2}(Vgs_1 - 0 - Vt_n)^2, \tag{2.27}$$

$$-Ids_3 = \frac{\beta_3}{2}(-Vgs_3 + Vt_p)^2 = \frac{\beta_3}{2}(-Vgs_1 + V_{dd} + Vt_p)^2. \tag{2.28}$$

with

$$Ids_2 = -Ids_3, \tag{2.29}$$

and

$$Vgs_1 = V_{sw}, \tag{2.30}$$

Equations 2.27 and 2.28 can be solved for V_{sw}, and yields

$$V_{sw} = \frac{V_{dd} + Vt_p + Vt_n\sqrt{\beta_2/\beta_3}}{1 + \sqrt{\beta_2/\beta_3}}. \tag{2.31}$$

The input current at which the inverter transitions from a logic high to a logic low can also be obtained, and from Equation 2.8 is given by

$$I_{sw} = \frac{\beta_1}{2}(V_{sw} - Vt_n)^2. \tag{2.32}$$

Therefore, with the exception of a current input, circuit behavior is similar to that of a standard CMOS inverter [Ref. 15].

4. Current Comparator

Another useful component is the current comparator. As shown in Fig. 2.5, this circuit is obtained from Fig. 2.4 by applying a constant reference voltage to the gate of transistor M_3. Its operation can be described in terms of a current-controlled

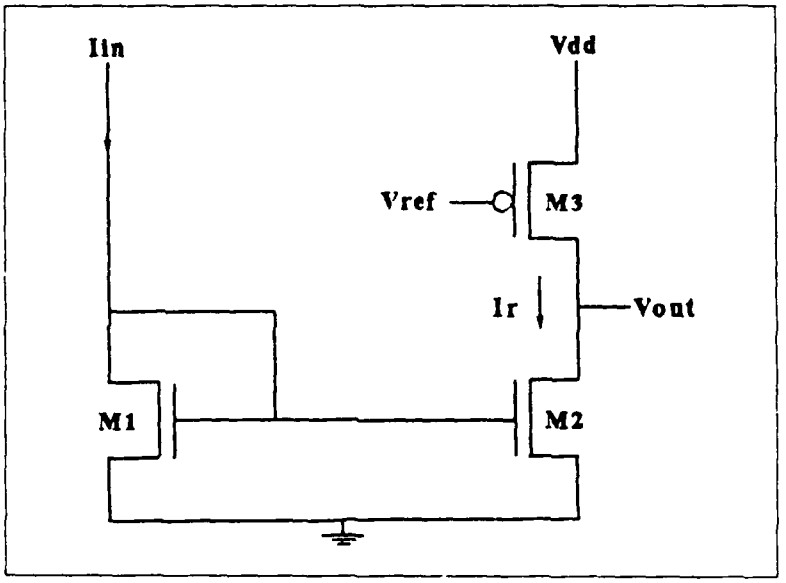


Figure 2.5: CMOS Current Comparator (After Ref. 13)

inverter, which yields:

$$V_{sw} = \frac{(V_{dd} - V_{ref}) + Vt_p + Vt_n\sqrt{\beta_2/\beta_3}}{1 + \sqrt{\beta_2/\beta_3}}, \tag{2.33}$$

and

$$I_{sw} = \frac{\beta_1}{2}(V_{sw} - Vt_n)^2. \tag{2.34}$$

However, another way to describe circuit operation is to consider I_r as the output of a current mirror and M_3 as an active current source [Ref. 13]. When viewed in this context, M_3 will function as either a dependent or constant current source, based on the value of I_r.

With I_{th} representing the saturation current of transistor M_3, when $I_r < I_{th}$, M_3 will operate as a current-controlled current source and will provide I_r on demand. From Equation 2.9, this current can be represented as

$$I_r = -Ids_3 = \beta_3[(-Vgs_3 + Vt_p)(-Vds_3) - \frac{(Vds_3)^2}{2}]. \tag{2.35}$$

Since

$$Vgs_3 = V_{ref} - V_{dd}, \tag{2.36}$$

and

$$Vds_3 = V_{out} - V_{dd}, \tag{2.37}$$

the current provided by M_3 in this region can be expressed as

$$I_r = \beta_3[(V_{dd} - V_{ref} + Vt_p)(V_{dd} - V_{out}) - \frac{(V_{dd} - V_{out})^2}{2}]. \tag{2.38}$$

If the restriction $\beta_1 = \beta_2$ is applied, then from Equation 2.23, $I_r = I_{in}$. Substituting this result into Equation 2.38 yields

$$I_{in} = \beta_3[(V_{dd} - V_{ref} + Vt_p)(V_{dd} - V_{out}) - \frac{(V_{dd} - V_{out})^2}{2}], \tag{2.39}$$

where we now have an expression that directly relates I_{in} to V_{out}. Solving this expression for V_{out} produces the more convenient form

$$V_{out} = (V_{ref} - Vt_p) + \sqrt{(V_{ref} - Vt_p)^2 - 2V_{dd}(V_{ref} - \frac{V_{dd}}{2} - Vt_p) - \frac{2I_{in}}{\beta_3}}. \tag{2.40}$$

and with V_{ref}, Vt_p, V_{dd} and β_3 considered constant for the design, an increase in I_{in} will produce a nonlinear decrease in V_{out} as expected in this region.

If I_{in} is increased to the point where $I_r = I_{th}$, then both M_2 and M_3 will operate in saturation. At this point, the comparator output voltage will transition from a logic high to a logic low. Since I_{th} is the maximum current M_3 can provide, further increases on I_{in} will not effect I_r and the comparator will remain a logic low. In this region, ($I_{in} \geq I_{th}$), M_3 operates as a constant current source, with its output given by

$$I_{th} = \frac{\beta_3}{2}(-Vgs_3 + Vt_p)^2 = \frac{\beta_3}{2}(V_{dd} - V_{ref} + Vt_p)^2. \tag{2.41}$$

From Equations 2.5, 2.9 and significant algebraic manipulation, an expression for the comparator output voltage in this region can also be obtained, and is given by

$$V_{out} = \frac{1}{\sqrt{\beta_2}}[\sqrt{2I_{in}} - \sqrt{2(I_{in} - I_{th})}]. \tag{2.42}$$

Therefore, when viewed in this context, circuit behavior can be described directly in terms of a current comparator, where the logic state of the device is determined from

$$V_{out} = \begin{cases} Logic\ \ HIGH & \text{for } I_{in} < I_{th} \\ Logic\ \ LOW & \text{for } I_{in} \geq I_{th} \end{cases} \tag{2.43}$$

It is also important to note that I_{th} can be set by varying the geometric parameters of transistor M_3 alone. As will later be shown, this characteristic is of particular interest for MVL applications.

5. Current Encoder

The final component of this section is the current encoder. As can be seen from Fig. 2.6, the circuit is composed of parallel branches, each of which contain an active current source and a pass transistor [Ref. 13]. The pass transistors are controlled by externally-supplied voltage signals (V_1 and V_2) and are used to connect or disconnect a particular current source from the encoder's output node. Each current source is set to provide one logical unit of current, which can be obtained

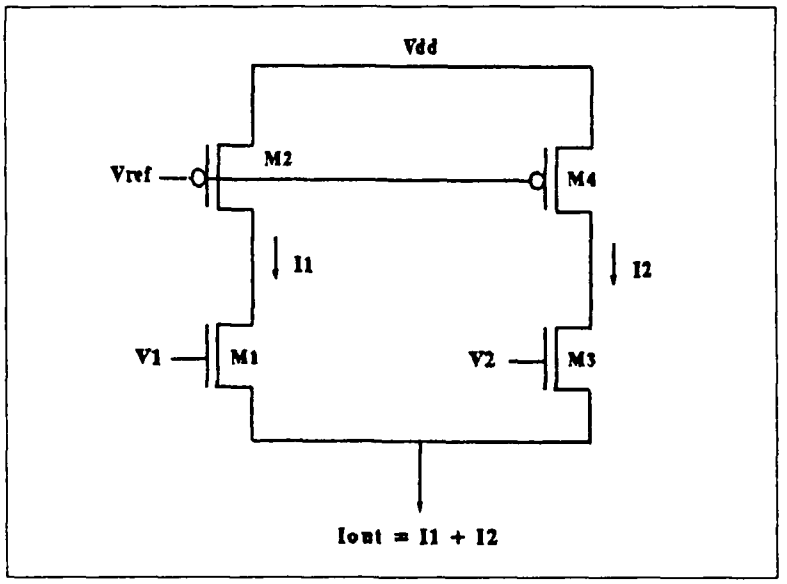


Figure 2.6: Three State CMOS Current Encoder (After Ref. 13)

from

$$I_{logic1} = \frac{\beta_p}{2}[V_{dd} - V_{ref} + Vt_p]^2, \quad for \quad V_{ref} < V_{dd} + Vt_p. \tag{2.44}$$

Since the final encoder output will be the sum of all applied branch currents, overall circuit behavior can be described as shown in Table 2.1.

TABLE 2.1: CURRENT ENCODER I/O CHARACTERISTICS

V_1	V_2	$Iout$
LOW	LOW	LOGIC 0
LOW	HIGH	LOGIC 1
HIGH	LOW	LOGIC 1
HIGH	HIGH	LOGIC 2

Although simple in construction, this is one of the few circuits that will provide logically restored current output signals for current-mode CMOS MVL applications.

III. AN EXISTING CURRENT-MODE CMOS DESIGN

This chapter describes an existing current-mode CMOS data latch. It is capable of storing four logic states and is the first of its kind known to exist. It was developed by K. W. Current at the University of California, Davis, and though specific references to his work may have been unintentionally omitted, the design concept is his alone.

A. OVERALL OPERATION

The first known hardware realization of a four-valued data latch was presented by K. W. Current in Ref. 13. The circuit is shown in Fig. 3.1 and though physical operation is not known to have been verified, SPICE simulations show promise of success.

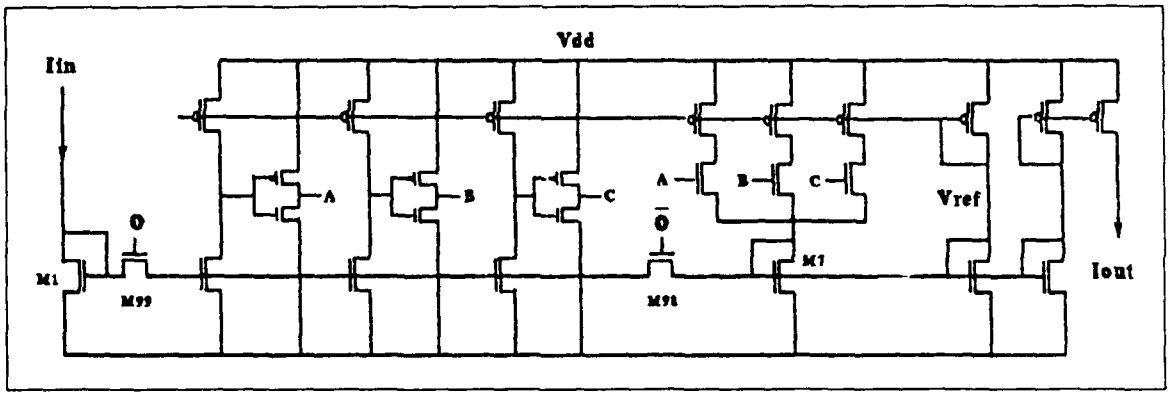


Figure 3.1: Four-Valued Current-Code CMOS Data Latch (After Ref. 13)

The latch is composed of three subcircuits: an input replicator, a multiple-valued-to-binary decoder and a binary-to-multiple-valued encoder. It has two modes of operation, setup and hold. When the clock signal ϕ is a logic high, the latch operates in the setup mode, and the input logic value is transmitted unchanged to the

output. The current I_{in} represents one of four possible logic states, and a comparator circuit is used to determine the input logic level actually present. Each leg of the comparator circuit performs a threshold operation on the input and produces output voltage signals V_A, V_B, and V_C. As shown in Table 3.1, the comparator outputs are binary and represent the input logic level in decoded format. [Ref. 13]

TABLE 3.1: COMPARATOR RESPONSE TO CURRENT INPUTS

I_{IN}	V_A	V_B	V_C
Logic 0	LOW	LOW	LOW
Logic 1	HIGH	LOW	LOW
Logic 2	HIGH	HIGH	LOW
Logic 3	HIGH	HIGH	HIGH

Each leg of the encoder subcircuit contains a pass transistor that either connects or isolates that leg from a common output node. The pass transistor is controlled by one of the comparator output voltages and for each high comparator output, one logical unit of current is presented to that node. The final encoder output is the sum of its individual branch currents, and this signal is replicated by the last subcircuit to form the latch output, I_{out}. [Ref. 13]

When the clock signal ϕ is a logic low, the latch operates in the hold mode. In this mode, the last logic input value is stored and held at the output. Specifically, I_{in} is disconnected from the circuit and the encoder output is provided (through a positive feedback loop) to the latch input. With the encoder providing a logically restored version of the original input signal, the latch state remains stable and will not be effected by the value of I_{in} until the next clock cycle occurs. [Ref. 13]

B. SELECTION OF THE REFERENCE VOLTAGE

Recall from Chapter II that current mode comparator and encoder subcircuits rely on a reference voltage for operation (see Figures 2.5 and 2.6). Since the storage device of this chapter is constructed from those circuits, two important design considerations are: 1) how to establish that reference voltage (V_{ref}); and, 2) what value of V_{ref} to select.

First, although V_{ref} could be provided by an external source, the routing of an additional inter-connection throughout the host IC chip would be required. Since additional inter-device connections directly lead to increased VLSI chip area, this method is undesirable and the auxiliary circuit of Fig. 3.2 is instead used to provide

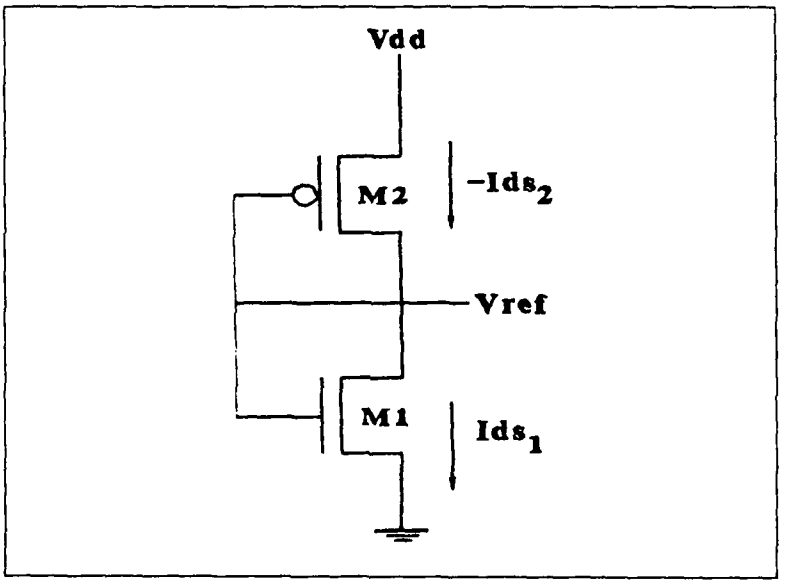


Figure 3.2: Reference Voltage Generator (After Ref. 13)

V_{ref} internally [Ref. 13]. Referring to Fig. 3.2, M_1 and M_2 are both diode-connected transistors. Assuming no current flow in the gate connections and in the lead marked V_{ref} yields,

$$-Ids_2 = \frac{\beta_2}{2}(V_{dd} - V_{ref} + Vt_p)^2 = \frac{\beta_1}{2}(V_{ref} - Vt_n)^2 = Ids_1. \qquad (3.1)$$

When solved for V_{ref}, we obtain

$$V_{ref} = \frac{V_{dd} + Vt_p + Vt_n\sqrt{\beta_1/\beta_2}}{1 + \sqrt{\beta_1/\beta_2}}, \tag{3.2}$$

which allows a wide range of reference voltages to be established by simply adjusting the geometric parameters of M_1 and M_2 alone. Equation 3.2 does not, however, provide insight to the value of V_{ref} that should be selected. To obtain this quantity, the behavior of the comparator subcircuit must first be considered.

From Equation 2.41, the threshold current for a single comparator leg can be expressed as

$$I_{th} = \frac{\beta_p}{2}(V_{dd} - V_{ref} + Vt_p)^2. \tag{3.3}$$

In addition, the comparator output voltage (V_{out}) is also a function of V_{ref}, and is obtained from Equations 2.40 and 2.42 as follows:

$$V_{out} = \begin{cases} \alpha + \sqrt{\alpha^2 - 2V_{dd}(\alpha - \frac{V_{dd}}{2}) - \frac{2I_{in}}{\beta_p}} & \text{for } I_{in} < I_{th} \\ \frac{1}{\beta_n}(2\sqrt{I_{in}} - \sqrt{2(I_{in} - I_{th})} & \text{for } I_{in} \geq I_{th} \end{cases}, \tag{3.4}$$

where $\alpha = V_{ref} - Vt_p$. From the above expressions, a family of input/output response curves for a single comparator leg can be obtained and a selection for V_{ref} can be made. As an example, I-V characteristics for a comparator leg (with $I_{th} = 5\ \mu$A) are shown in Fig. 3.3. These curves were obtained from Equation 3.4, where Equation 3.3 was used to determine the transistor gain factor (β_p) required to achieve the 5 μA threshold current for each value of V_{ref} that was selected.

As can be seen from Fig. 3.3, the higher the reference voltage, the sharper the transition from a logic high to a logic low on the comparator output. This is desired because of superior discrimination between input logic levels. However, when $I_{in} = I_{th}$ at high values of V_{ref}, the comparator output voltage has a large transition to make before achieving its complement logic state. This is synonymous with increased delay time. At low values of V_{ref}, delay times are minimized, but this is accompanied by

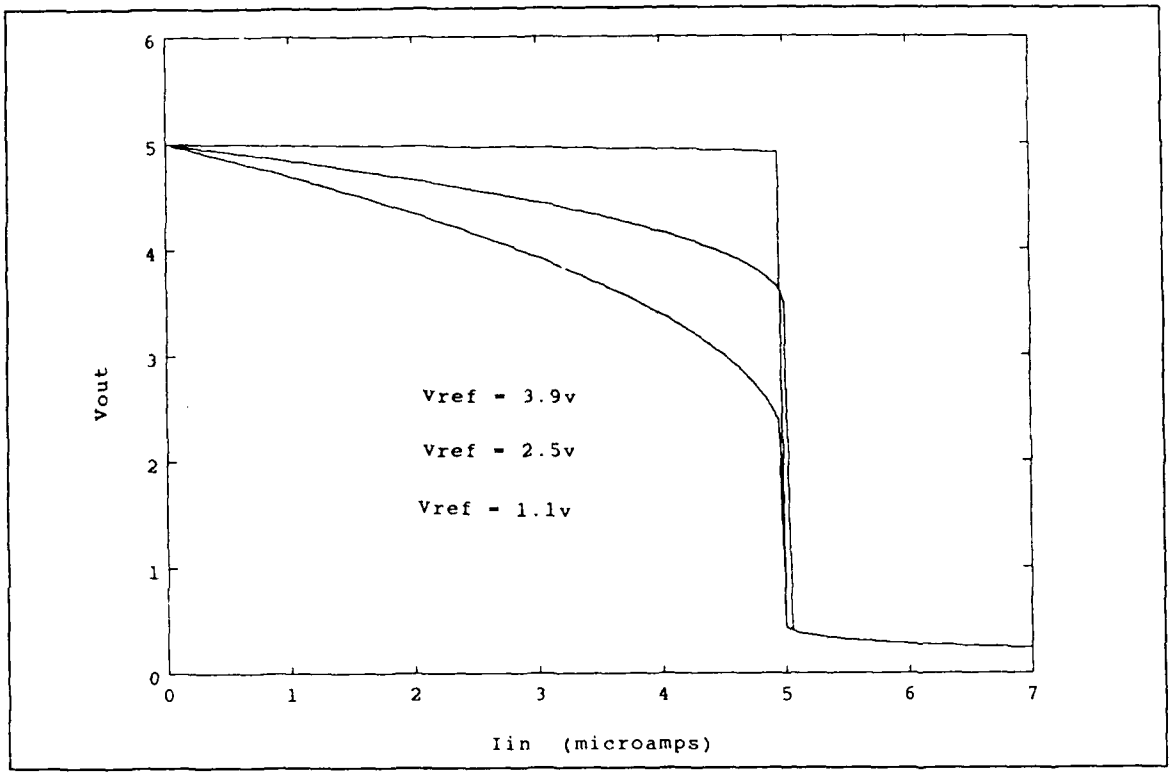


Figure 3.3: Comparator Leg I-V Characteristics

poor input logic level discrimination. In addition, maintaining specific comparator leg threshold currents requires unreasonably large transistor geometries at either of the reference voltage extremes. Therefore, as a compromise between conflicting requirements, a value of $V_{ref} = V_{dd}/2$ was selected for the initial design attempt of this study. Although significantly lower than suggested by Ref. 13, several advantages are obtained through the use of a lower V_{ref}. These will become apparent as the operational characteristics of each subcircuit are presented.

With $V_{dd} = 5$ V, $Vt_n = 0.62$ V, $Vt_p = -0.84$ V and process dependent parameters K_n and K_p given by Appendix A, Equation 3.2 can be used to obtain β_n/β_p. For a reference voltage of 2.5 V, this yields

$$\frac{\beta_n}{\beta_p} = \frac{K_n}{K_p}\left(\frac{W_n/L_n}{W_p/L_p}\right) = 0.780, \tag{3.5}$$

or

$$\frac{W_n/L_n}{W_p/L_P} = 0.242. \tag{3.6}$$

A unique solution does not exist for selecting final transistor geometries; however, a stable reference voltage is required and static power consumption should be kept to a minimum. From PSPICE trial and error simulations [Ref. 16], the combination of

$$\frac{W_n/L_n}{W_p/L_p} = \frac{3\lambda/33\lambda}{3\lambda/8\lambda}, \tag{3.7}$$

where $\lambda = 1.5$ microns, provides a reference voltage of 2.51 V at a current flow of approximately 8.7 μA. Attempts to further reduce the current flow through transistors M_1 and M_2 of Fig. 3.2 either result in unsatisfactory reference voltage oscillations or unreasonably large transistor dimensions. Therefore, the width-to-length ratios shown in Equation 3.7 were selected as the final transistor geometries for this design.

As the first advantage of using a lower reference voltage,

$$\frac{W_n/L_n}{W_p/L_p} = \frac{3\lambda/42\lambda}{17\lambda/2\lambda}, \tag{3.8}$$

was found to produce $V_{ref} = 3.76$ V, and a current flow of approximately 17.7 μA. With only two diodes in the circuit of Fig. 3.2, further current flow reductions are extremely difficult to achieve without lowering V_{ref}. As can be seen, this is almost twice the current; and therefore, twice the static power consumption of the previous example.

C. THE COMPARATOR SUBCIRCUIT

The comparator subcircuit of Fig. 3.4 decodes the input logic level (as shown in Table 3.1) and provides three binary control signals to the encoder subcircuit for input

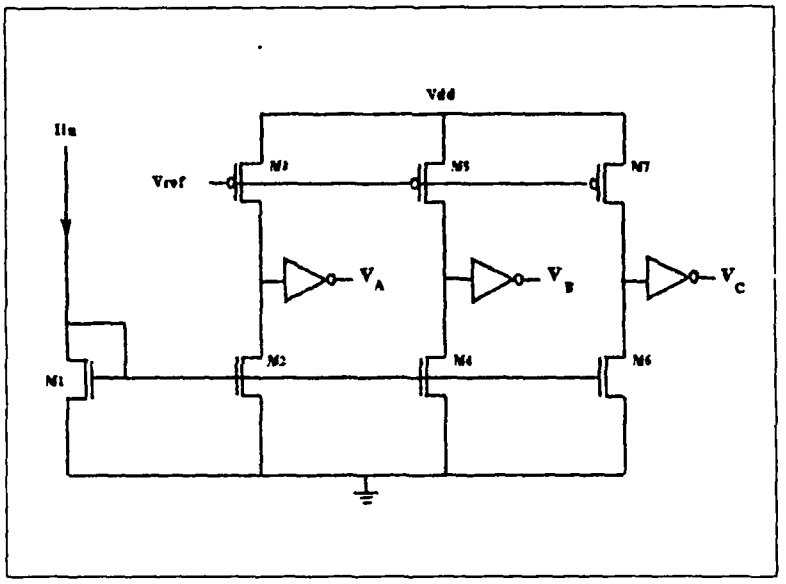


Figure 3.4: The Comparator Subcircuit (After Ref. 13)

logic level restoration [Ref. 13]. As described in Chapter II, each of the comparator leg output voltages ($\overline{V}_A$, $\overline{V}_B$, and $\overline{V}_C$) depend on the value of the threshold current set for that leg. As an example, if the active current source M_3 is set to provide a threshold current of $I_{th} = I_{logic1}$, then $\overline{V}_A$ will be a logic high for $I_{in} < I_{logic1}$ and a logic low for $I_{in} \geq I_{logic1}$.

To minimize static power requirements, I_{in} is limited to a maximum of 30 μA. Logic states 0, 1, 2 and 3 are defined as 0, 10, 20 and 30 μA, respectively [Ref. 13]. Although the midpoint between each logic level is the preferred threshold, lambda-based design rules make the 25 μA threshold difficult to achieve. As a result, comparator leg thresholds were selected as 5, 15 and 24 μA [Ref. 13].

To set the thresholds, a modified form of Equation 2.41 can be used:

$$Ith_{mi} = \frac{\beta_{mi}}{2}(V_{dd} - V_{ref} + Vt_p)^2 = \frac{K_p W_{mi}}{2\ L_{mi}}(V_{dd} - V_{ref} + Vt_p)^2, \qquad (3.9)$$

where mi = transistor M_3, M_5 or M_7. The required W/L ratio for each threshold can therefore be obtained from

$$\left(\frac{W_{mi}}{L_{mi}}\right) = \frac{2(Ith_{mi})}{K_p(V_{dd} - V_{ref} + Vt_p)^2}. \qquad (3.10)$$

For a $\lambda = 1.5$ micron process, only discrete transistor dimensions (in increments of 1.5 microns) are allowed. Therefore, transistor widths and lengths must be selected to approximate (W_{mi}/L_{mi}) as closely as possible, while preventing either of the dimensions from becoming unreasonably large. With V_{ref} set at 2.51 V, Table 3.2 summarizes the results of the above calculations.

TABLE 3.2: COMPARATOR CURRENT SOURCE TRANSISTOR GEOMETRIES

comparator leg	current source	desired Ith	calculated β_p	calculated W_p	calculated L_p	actual β_p	actual W_p	actual L_p
1	M_1	5 μA	0.171	4λ	17λ	0.136	3λ	22λ
2	M_3	15 μA	0.513	3λ	6λ	0.625	5λ	8λ
3	M_5	24 μA	0.823	9λ	11λ	1.0	4λ	4λ

Note that the ideal transistor model, which was used to obtain Equation 3.10, only provides a first approximation for the necessary transistor geometries. Although a more complete mathematical model would provide better initial estimates, obtaining final transistor geometries still requires significant SPICE trial-and-error simulations. As a result, the complexity of dealing with a more accurate transistor model was considered beyond the point of diminishing returns and the results of Equation 3.10 were used directly in the PSPICE simulation program [Ref. 16]. Transistor dimensions

resulting from this trial and error process have also been included in Table 3.2, and as can be seen, the ideal transistor model performs poorly in this application.

Transistor M_1 (in conjunction with M_2, M_4 and M_6), forms a current mirror with each of the three comparator legs. As described in Chapter II, for a current mirror to reflect $I_r = I_{in}$, the NMOS transistor gain factors must be equal (see Equation 2.23). As a result, we require

$$\beta_{mi} = \beta_n = \frac{K_n}{2}(W_n/L_n), \tag{3.11}$$

where i = 1, 2, 4 or 6. Since the current mirrors perform the same function in this circuit as in the comparator of Chapter II, a detailed analysis will not be repeated here. However, in an attempt to minimize circuit area, dimensions W_n and L_n were selected as 3λ and 2λ respectively. These represent the minimum transistor dimensions for lambda-based design rules.

PSPICE simulations for this portion of the circuit reveal the purpose of the inverters on the output of each comparator leg. As can be seen from Fig. 3.5, as the comparator input current is increased, the comparator leg output voltages successively transition from a logic high to a logic low. With 2.5 V defined as the point at which this transition occurs, examination of the above plot shows that the logic shifts closely correspond to comparator input currents of 5, 15 and 24 μA as desired. Since the comparator outputs will be used as binary control signals, a much sharper response from one logic level to another is preferred. To provide this type of response, a standard CMOS inverter is placed on the output of each comparator leg [Ref. 13]. As can be seen from Fig. 3.6, although delay is introduced by the presence of the inverters, the transition from one logic state to another is much sharper. These inverted signals (V_A, V_B and V_C in Fig. 3.6) are now the binary control signals previously referred to in Table 3.1.

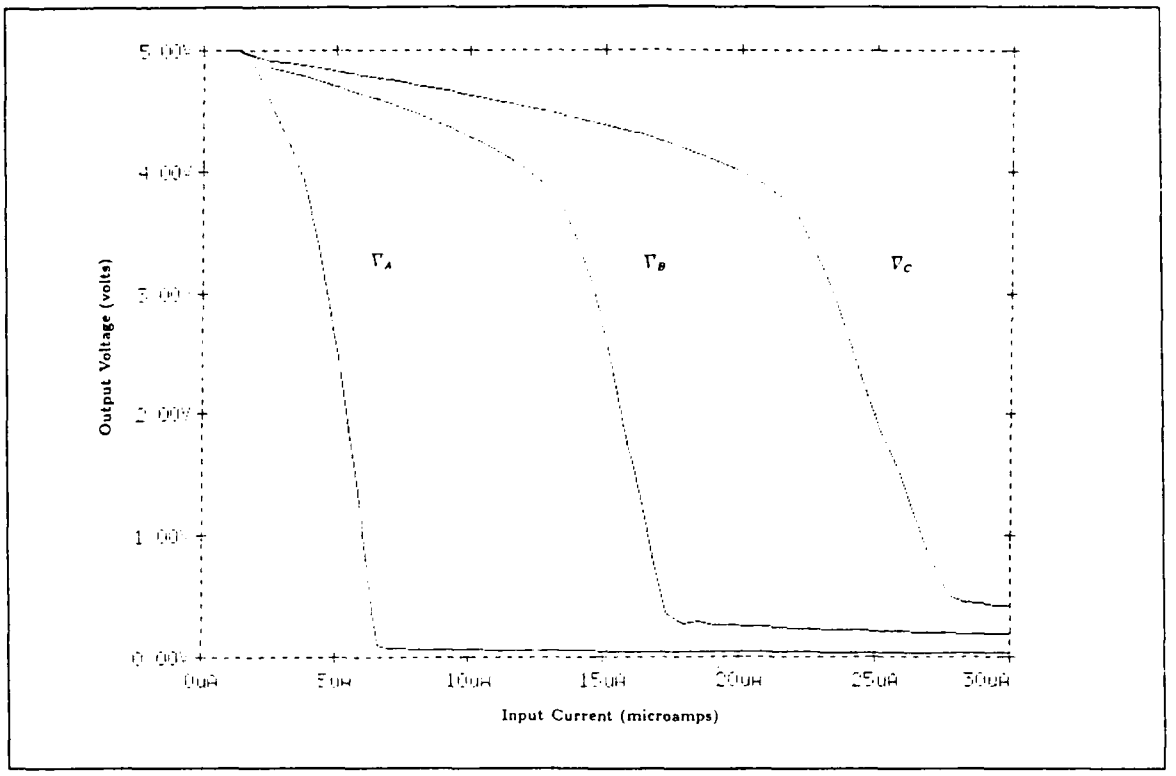


Figure 3.5: Comparator Leg Response to a Ramped Input Current

It should be noted that the transistor geometries of Table 3.2 result in significantly lower width-to-length ratios than that provided by Ref. 13. However, one problem encountered during PSPICE simulations of the comparator network using higher width-to-length ratios was an undesirable sensativity to the rate at which I_{in} was allowed to change. When the comparator threshold currents were set using DC analysis, circuit operation in transient analysis required input currents in excess of the original thresholds to achieve comparator leg output voltage transitions. Reference 17 briefly addresses the problem and notes that higher output impedance cascode current sources are used in the actual latch design to minimize this effect (Fig. 3.1 is a simplified schematic). Since this significantly contributes to circuit complexity, that method was not pursued. Instead, it was noted that a lower reference voltage also reduces comparator leg sensitivity. With V_{ref} low, threshold currents can be generated

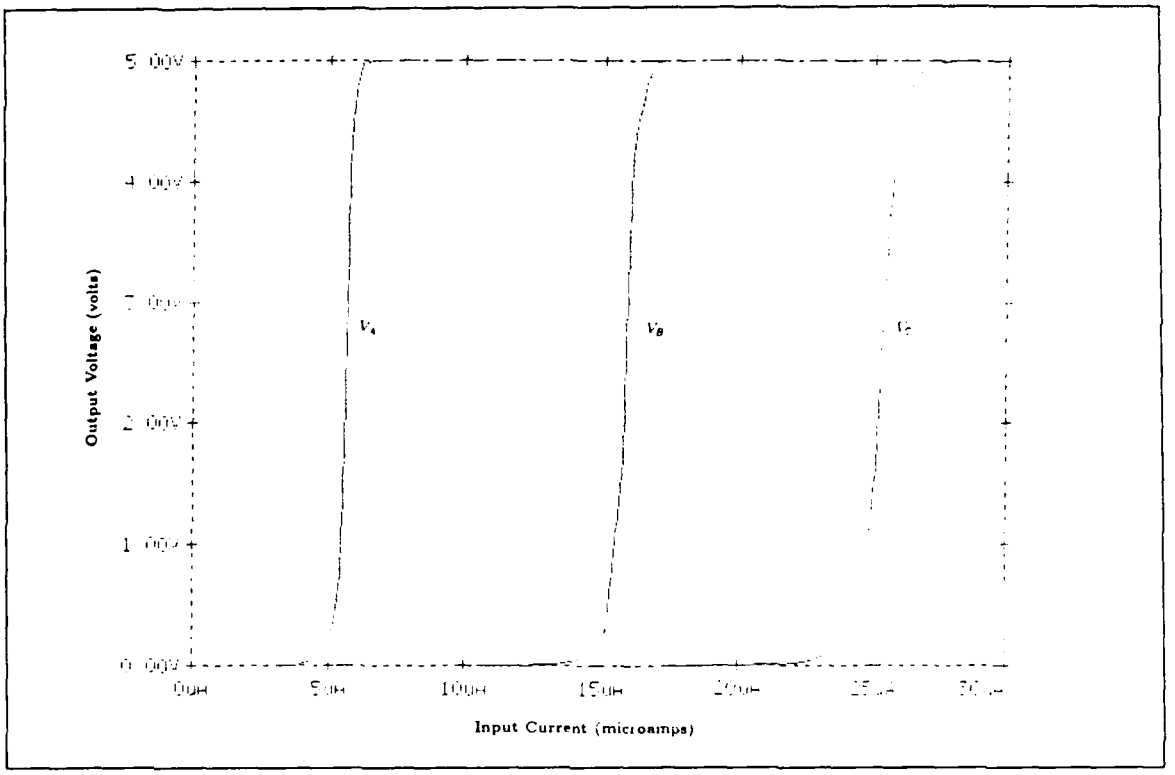


Figure 3.6: Comparator Output Control Signals V_A, V_B, V_C

using reduced PMOS transistor gain factors (β_p). Although this does not solve the problem, it appears to minimize its effect on PSPICE transient latch operations. As will be shown in the next section, gradual comparator logic transitions resulting from the lower reference voltage selection may not be altogether undesirable.

D. THE ENCODER SUBCIRCUIT

The purpose of the encoder subcircuit is to convert the three binary control signals (V_A, V_B and V_C of Fig. 3.4) into a single, logically-restored four-valued signal. Shown in Fig. 3.7, each of the encoder's active current sources (M_4, M_5 and M_6) are set to provide one logical unit of current to a summing junction, as controlled by pass transistors M_1 through M_3. Following the same procedure used to obtain comparator thresholds, each active current source is set to provide 10 μA. For $V_{ref} = 2.51$ V, this

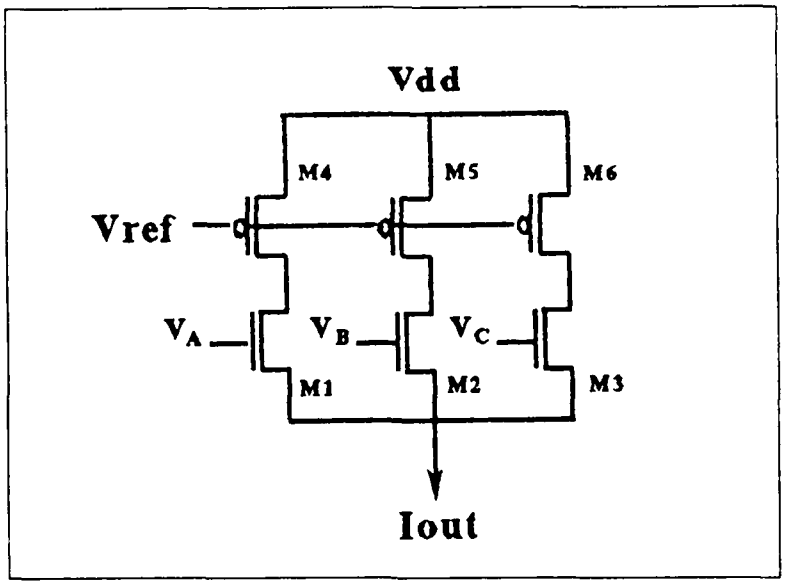


Figure 3.7: The Encoder Subcircuit (After Ref. 13)

requires M_4, M_5 and M_6 to be dimensioned at $W_p/L_p = 3\lambda/7\lambda$. Although minimum dimensions for the NMOS pass transistors were initially thought to be preferred, increased transistor lengths were selected to reduce current spikes that occur when the pass transistors bias on. To illustrate the severity of this effect, a single branch of the encoder circuit was isolated, as shown in Fig. 3.8, and PSPICE simulations were performed using an ideal voltage source to control its pass transistor. With M_1 set at minimum lambda dimensions, Fig. 3.9 shows a current spike of approximately 120 μA; which is 110 μA above the current source's output. Since Kirchhoff's current law appears to be violated, this requires further explanation.

Shown in Figures 3.10a, 3.10b and 3.10c are the drain, gate and substrate contributions to the final current that M_1 provides to the encoder output summing junction. If M_1 and M_3 performed as predicted by the ideal transistor model, a current flow of 10 μA would be provided. However, as can be seen from Fig. 3.10, significant contributions to the encoder output current are provided by non-ideal transistor characteristics as well. PSPICE simulations suggest each of these contributions are a

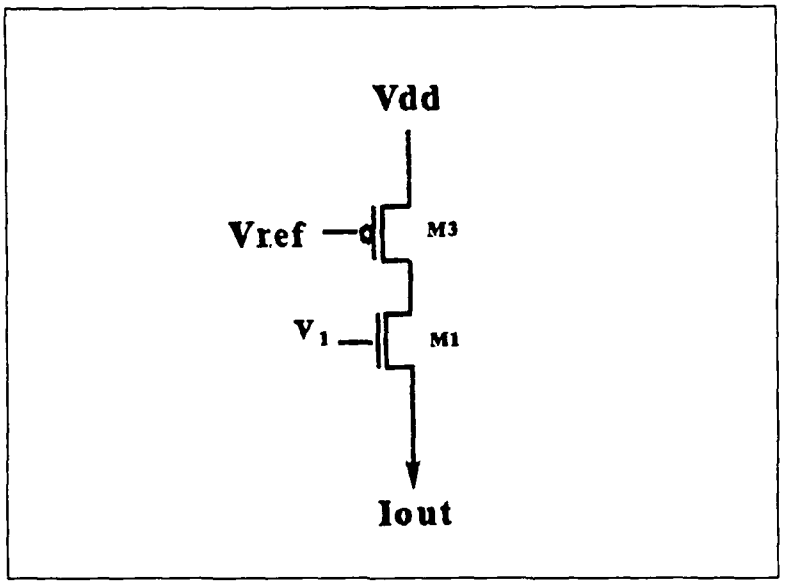


Figure 3.8: An Encoder Test Circuit

direct result of the parasitic capacitances inherent in a MOSFET transistor, some of which are shown in Fig. 3.11. It is interesting to note that when these capacitances (as well as parasitic capacitance on the device interconnections) are removed, current spikes are no longer present on the encoder output.

When V_1 is at a logic low (see Fig. 3.8), the drain, gate and source of M_1 are at V_{dd}, ground and Vt_n respectively. As V_1 transitions to its logic high state, M_1 will bias on, current will flow through the device, and each of the above voltages will rapidly change. Since current through a capacitor is described by $I_c = CdV/dt$, this gives rise to the short-duration current spikes shown in Fig. 3.10.

In Fig. 3.10a, although parasitic capacitance in transistor M_1 has an effect, PSPICE simulations indicate the primary contribution to this current spike comes from transistor M_3. With the drains of M_1 and M_3 connected, when M_1 biases on, both transistor drain voltages drop sharply. This develops a voltage V_{bd} between the drain of M_3 and the substrate on which it is fabricated. With PMOS devices having V_{dd} applied to their substrate connection, a current $I_c = (C_{bd})dV_{bd}/dt$ will flow

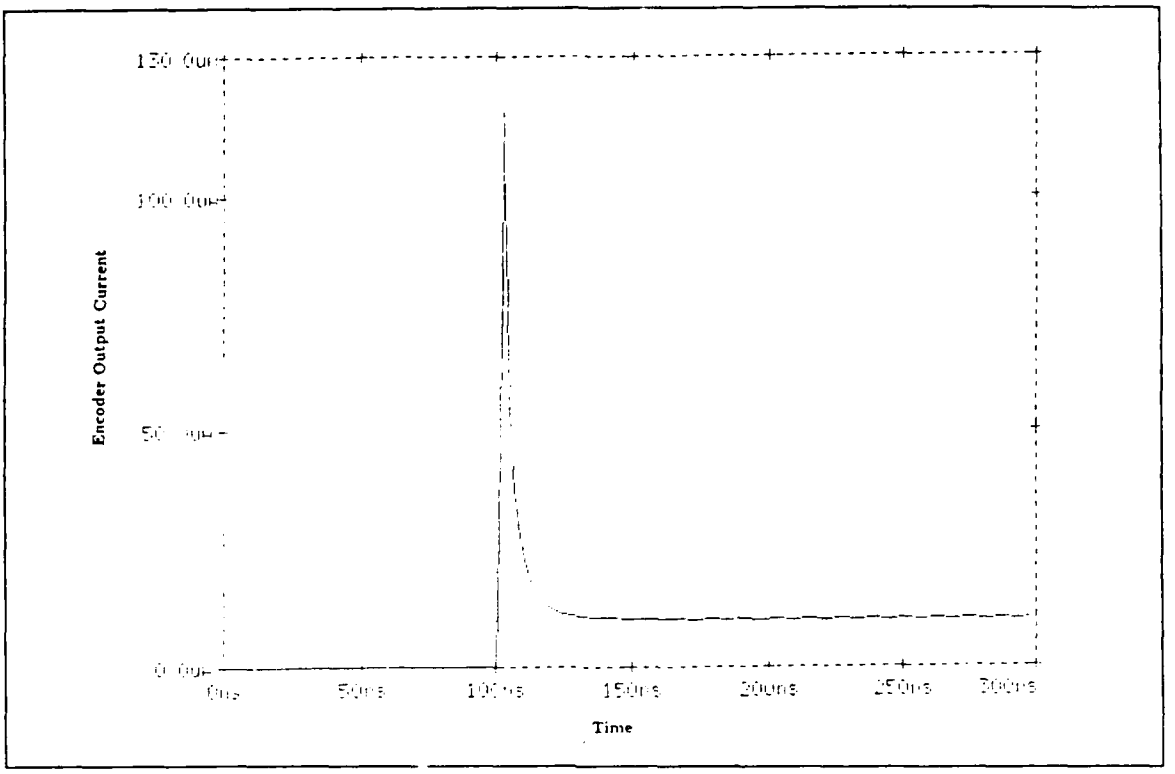


Figure 3.9: Encoder Test Circuit Output

from the substrate to the drain of the device. As can be seen from Fig. 3.10a, this contribution can be significant.

In Fig. 3.10b, as V_1 transitions from logic low to logic high, parasitic capacitance between the gate and source of M_1 also provides a short-duration current contribution to the encoder's output. Although not as large as the spike from transistor M_3, its magnitude is still approximately three times greater than predicted by the ideal transistor model.

In Fig. 3.10c, since the substrate connection of an NMOS device is set at the ground potential, as the source voltage of transistor M_1 raises, the substrate removes current from its output. Although desirable for this application, the magnitude of this current is insufficient to cancel the positive current contributions described above. As a result, a significant current spike will be presented to the encoder output as each

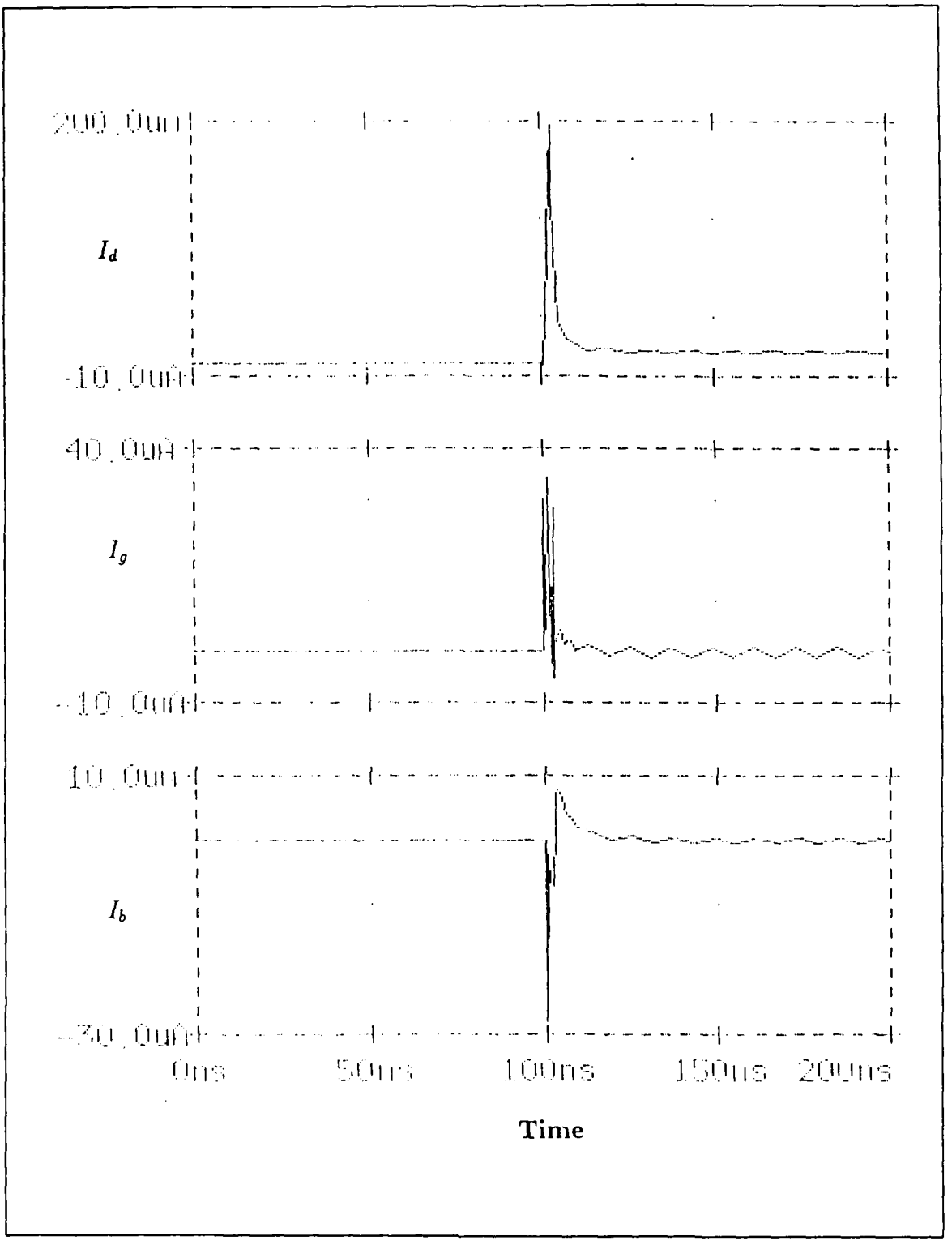


Figure 3.10: Individual Contributions to Encoder Output Current Spikes

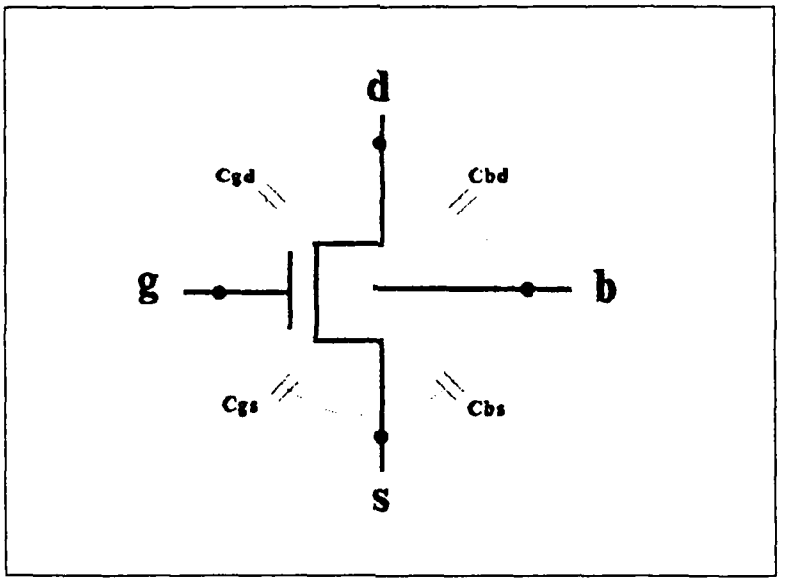


Figure 3.11: Parasitic Capacitance in a MOSFET Transistor

pass transistor biases on. When parasitic capacitance for device interconnections are also included, the example transient current of Fig. 3.9 becomes the final result.

Although the current spikes do not appear to affect overall latch operation, their presence is a major source of concern for the performance of downstream logic circuitry. In addition, minimizing their effect without unnecessarily increasing latch delay is a significant design challenge. As an example, parasitic capacitance can be added to the summing junction of Fig. 3.7. This will limit the magnitude of the spike but results in the encoder's output remaining above higher logic level threshold currents for a longer period of time. Since the encoder output provides the feedback signal to the comparator network (see Fig. 3.1), this could result in a loss of logic state when the latch transitions from its setup to hold mode of operation. This is unacceptable. As a compromise between increased latch delay and decreased current spike magnitude, two methods were found to produce acceptable results.

First, increasing the length of the pass transistors decreases their gain factor β_n. This results in a slower transistor response to sudden current oscillations. Second,

as noted in the previous sections, a lower reference voltage allows the comparator leg output to drop gradually as I_{in} approaches the comparator leg's threshold current. With the comparator output gradually decreasing, its downstream inverter will also make a more gradual change between logic states. Since this decreases dV/dt on the gate of the pass transistor, this also decreases the capacitive current contributions provided to the encoder output.

E. FORMING THE OUTPUT

Since a path to ground must be present for current to flow, the output of the encoder subcircuit is connected to transistor M_7 as shown in Fig. 3.12. For proper latch operation, this current (I_F) must not be interrupted, (or corrupted), by external

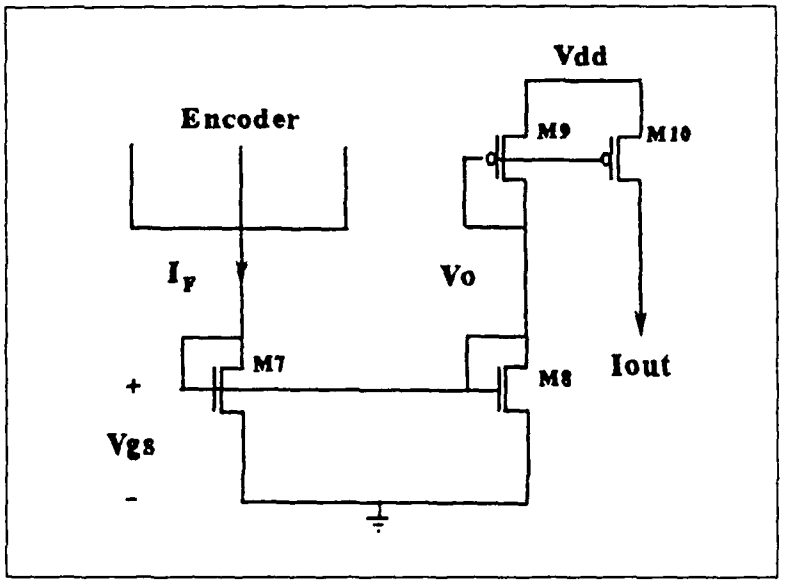


Figure 3.12: The Output Subcircuit (After Ref. 13)

sources. Therefore, a current mirror is required to reflect I_F onto the latch output.

When $I_F > 0$, a voltage (Vgs) will be developed across transistor M_7. When this voltage is above Vt_n for transistor M_8, M_8 will operate in saturation. Since M_9 is a diode-connected transistor, the current flowing through each of these devices can

be expressed as

$$-Ids_9 = \frac{\beta_9}{2}(V_{dd} - V_0 + Vt_p)^2 = \frac{\beta_8}{2}(Vgs - Vt_n)^2 = Ids_8. \tag{3.12}$$

From this equation, the voltage V_0 can be obtained and is given by

$$V_0 = V_{dd} - \sqrt{\frac{\beta_8}{\beta_9}}(Vgs - Vt_n) + Vt_p. \tag{3.13}$$

With the gate of transistor M_{10} connected to V_0, M_{10} becomes an active current source. In this application, V_0 is no longer a constant reference voltage; and as a result, the saturation current provided by M_{10} will also be variable:

$$-Ids_{10} = \frac{\beta_{10}}{2}(V_{dd} - V_0 + Vt_p)^2. \tag{3.14}$$

With V_0 given by Equation 3.13 and Vgs obtained from

$$Vgs = \sqrt{\frac{2I_F}{\beta_7}} + Vt_n, \quad for \quad I_F \geq 0, \tag{3.15}$$

substitution into Equation 3.14 yields

$$-Ids_{10} = \left(\frac{\beta_8\beta_{10}}{\beta_7\beta_9}\right) I_F = I_{out}. \tag{3.16}$$

For equally dimensioned transistors, $\beta_7 = \beta_8$, $\beta_9 = \beta_{10}$ and the desired result

$$I_{out} = I_F \tag{3.17}$$

is obtained. In actual PSPICE simulations, the voltage developed across transistor M_7 is slightly higher than that predicted by Equation 3.15 above. As a result, this current mirror operates with a gain factor slightly greater than unity. In addition, Vgs is not a linear function of I_F, and the output of the current mirror will not replicate its input throughout the entire region of operation. To compensate for both effects, the width of transistor M_8 was increased to 4λ while M_9 and M_{10} were maintained at minimum dimensions. Although not a unique solution, latch outputs resulting from the above modification are favorable. This will be shown in the section that follows.

F. OVERALL CIRCUIT SIMULATIONS

For the convenience of presenting the simulation results of this section, Fig. 3.1 has been reproduced as Fig. 3.13 below. In addition, the PSPICE data file required

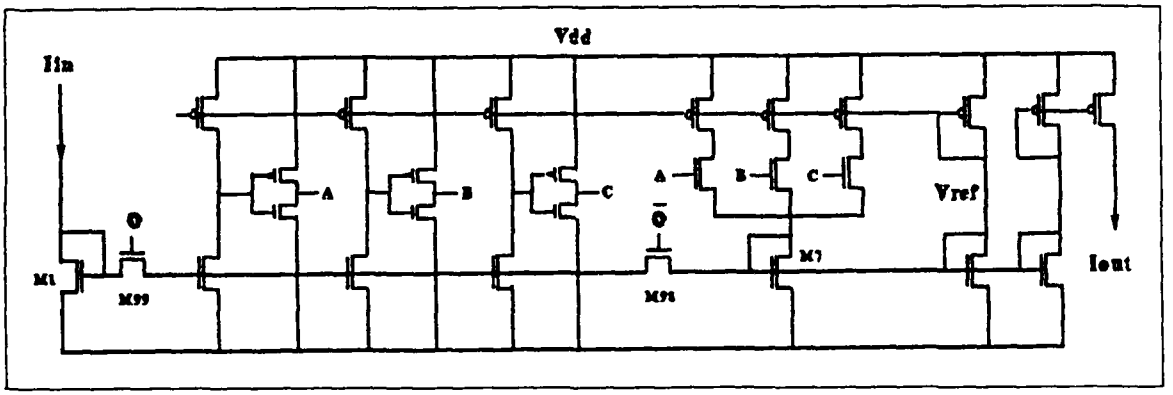


Figure 3.13: Four-Valued Current-Mode CMOS Data Latch (From Ref. 13)

for this circuit has been included in Appendix B for reference. It should be noted, however, that one of the most difficult simulation problems for this circuit occurs when the encoder-comparator positive feedback loop is incorporated into the design. Without assistance, PSPICE will not converge. Although the SPICE user's guide addresses this problem [Ref. 18], neither of the two recommended solutions were found to be successful. However, for each case that PSPICE failed to converge, the most erratic node voltage consistently appeared on the encoder side of transistor M_{98} in Fig. 3.13. As a result, the PSPICE initial condition card was used to set this node to Vt_n, which eliminated further convergence problems. Although the initial condition constraint is automatically removed during transient analysis [Ref. 18] to ensure it does not effect circuit operation, at least 100 ns are allowed to pass before dramatic changes on the input are allowed to occur.

With convergence problems resolved and each of the individual subcircuits incorporated into the design (see Fig. 3.13), the first simulation required is to verify circuit operation in the setup mode. With clock signal ϕ fixed at a logic high, the

latch's response to a slowly ramped input current is provided by Figures 3.14a and 3.14b. As can be seen from Fig. 3.14a, input logic level discrimination by the comparator subcircuit still occurs at the desired thresholds, and though current spikes are still present, Fig. 3.14b provides the desired overall input/output characteristics.

To verify operation in the hold mode, the ramped input current used in the previous simulation is applied to the latch in the setup mode to a maximum of 10 μA. At this point, the clock signal ϕ transitions from a logic high to a logic low and places the latch in its hold mode of operation. As can be seen from Fig. 3.15, latch operation in the the hold mode is satisfactory, however, the same effect that produces the encoder pass transistor current-spikes is also present for the clock pass transistors.

To determine delay times, Figures 3.16a, 3.16b and 3.16c show circuit response to a step input of 10, 20 and 30 μA respectively. Although Ref. 13 claimed worst case setup and hold times of 40 ns for the logic 0-to-3 and 3-to-0 transitions, these results could not be reproduced. (Recall, however, that Ref. 13 notes this latch is a simplified version of the final design). As can be seen from Fig. 3.16a, the logic 0-to-1 and 1-to-0 transitions present the worst case delay times for the latch of 105 ns and 115 ns respectively. This is contrary to the expected result and is due to the operational characteristics of the diode-connected transistors M_1 and M_7 (see Fig. 3.13).

Figures 3.17 and 3.18 provide the voltage (Vgs) developed across transistors M_1 and M_7 as a function of time. To obtain these curves, the three stepped input signals used to determine the latch delay times in the previous figures were again used for this example, with the results superimposed onto one plot. For the step up transitions, with I_{in} at 0 μA, the diode-connected transistor M_1 is in cutoff. From this state, the rate at which I_{in} is applied to the drain of the device determines the rate at which Vgs increases toward its steady state value (see Fig. 3.17). This affects the rate at which the comparator responds to Iin as well. As a result, higher step

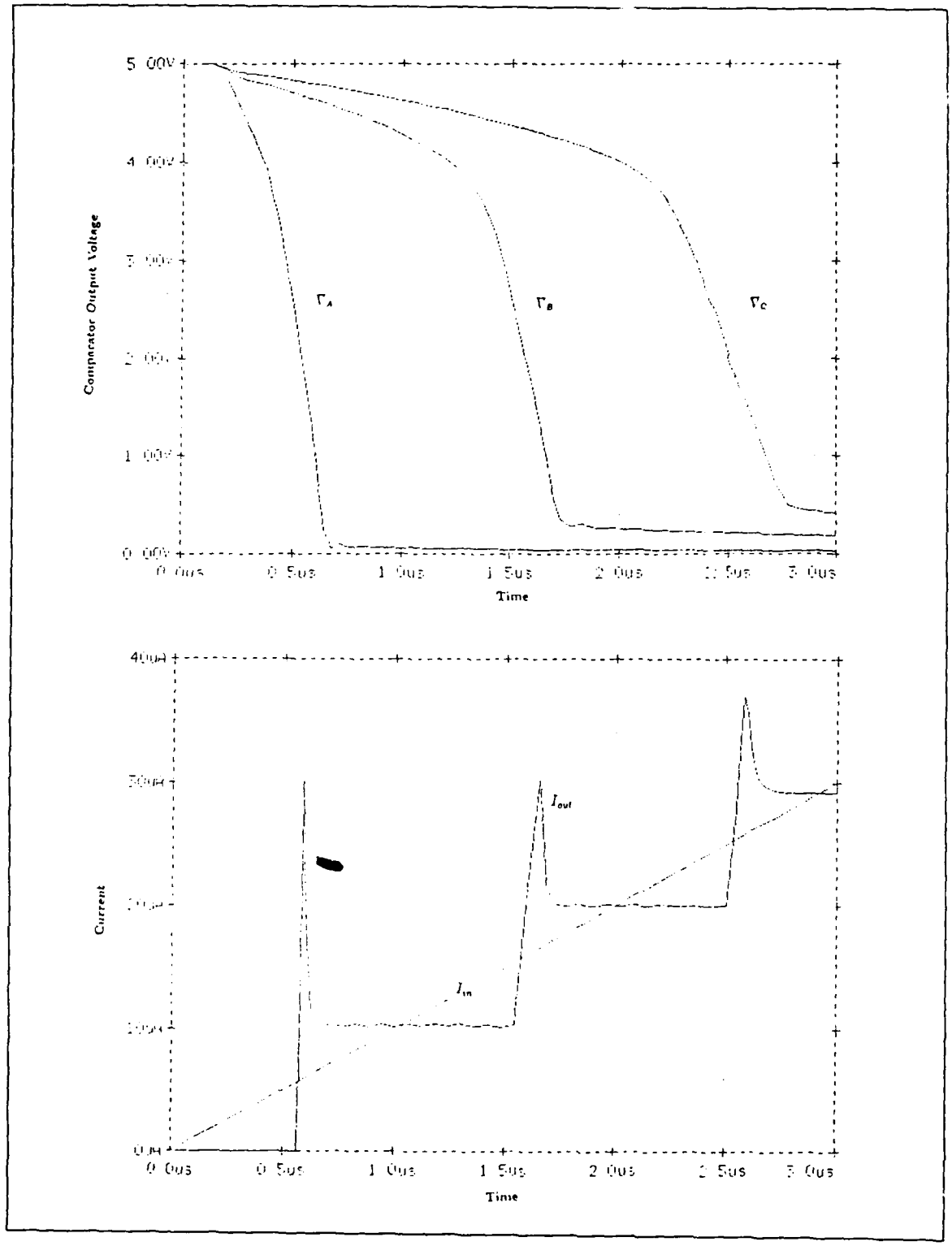


Figure 3.14: Circuit Response in the Setup Mode

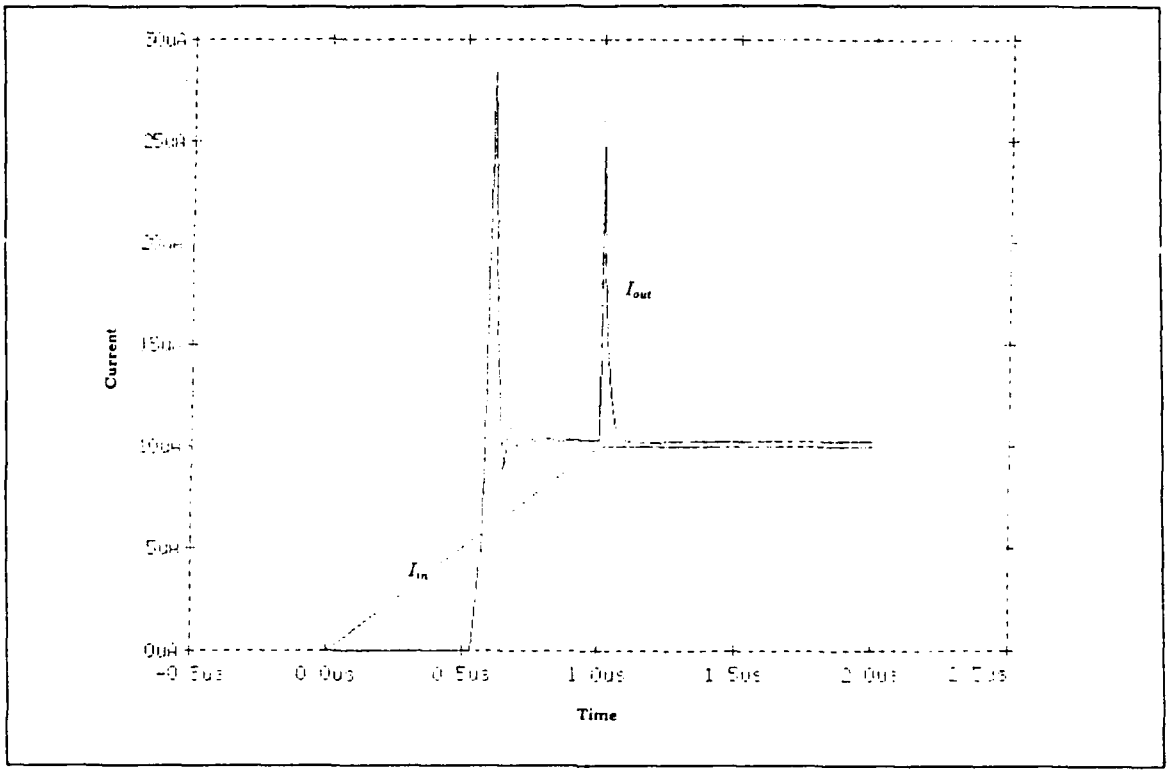


Figure 3.15: Latch Output in the Hold Mode

input currents produce faster comparator response times; and therefore, less delay throughout the circuit.

For the step-down transitions, a $1/RC$ time constant decay from the initial Vgs back to the cutoff voltage (Vt_n) is experienced by transistor M_7, (see Fig. 3.18). Although this does not present a problem for the logic 3- or logic 2-to-0 transitions, a significant delay is experienced while the device attempts to discharge the voltage corresponding to a logic 1 latch state. This is due to the exponential rate of decrease in Vgs from the logic 1-to-0 state. As a result, each step-down transition "hangs" at the logic 1 state for a long period of time.

Reference 17 notes that a bias current of one-half a logic current increment was added to the final design to keep these transistors biased on; and therefore, improve their speed performance. However, attempts to use this approach in the simplified

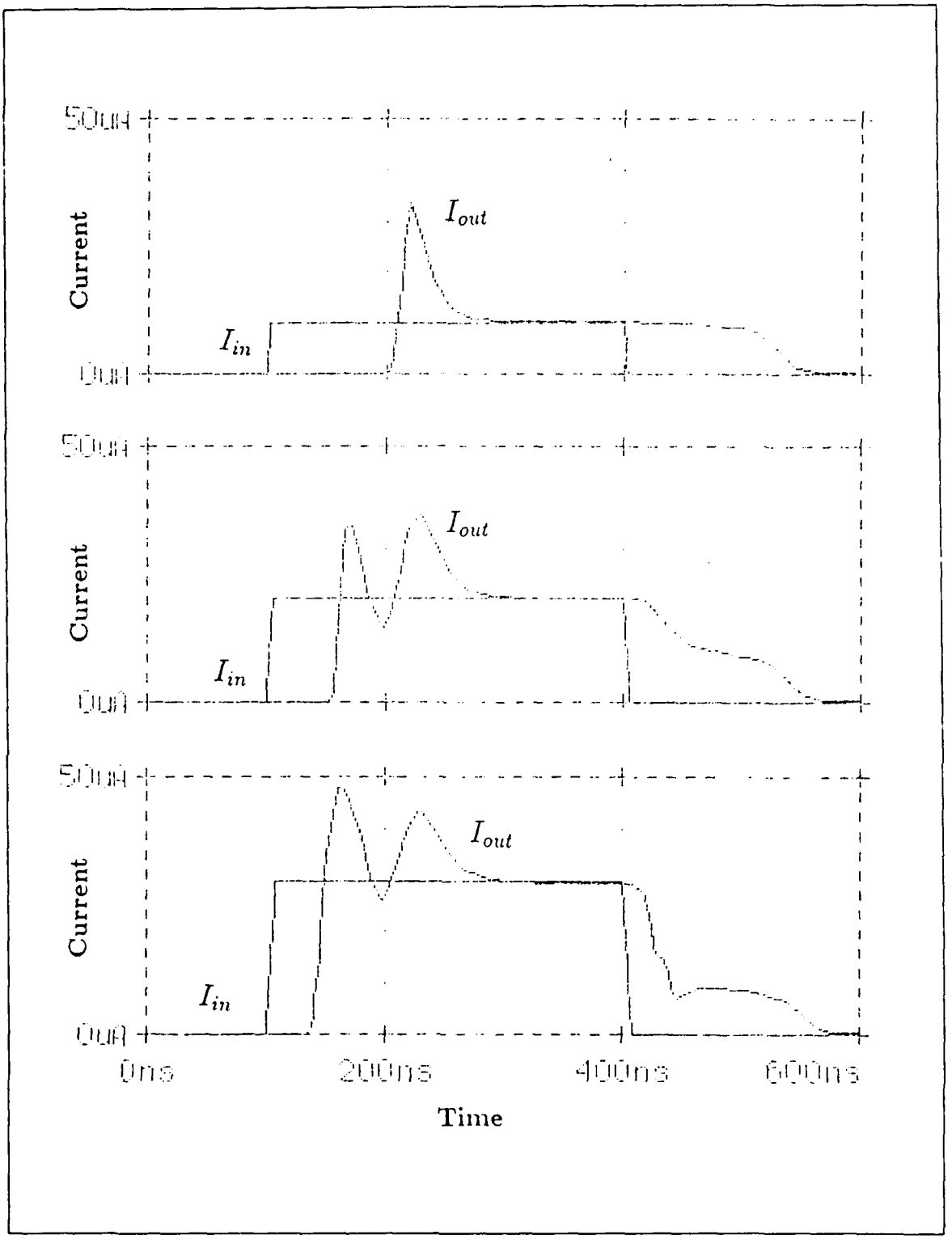


Figure 3.16: Latch Response to Step Inputs

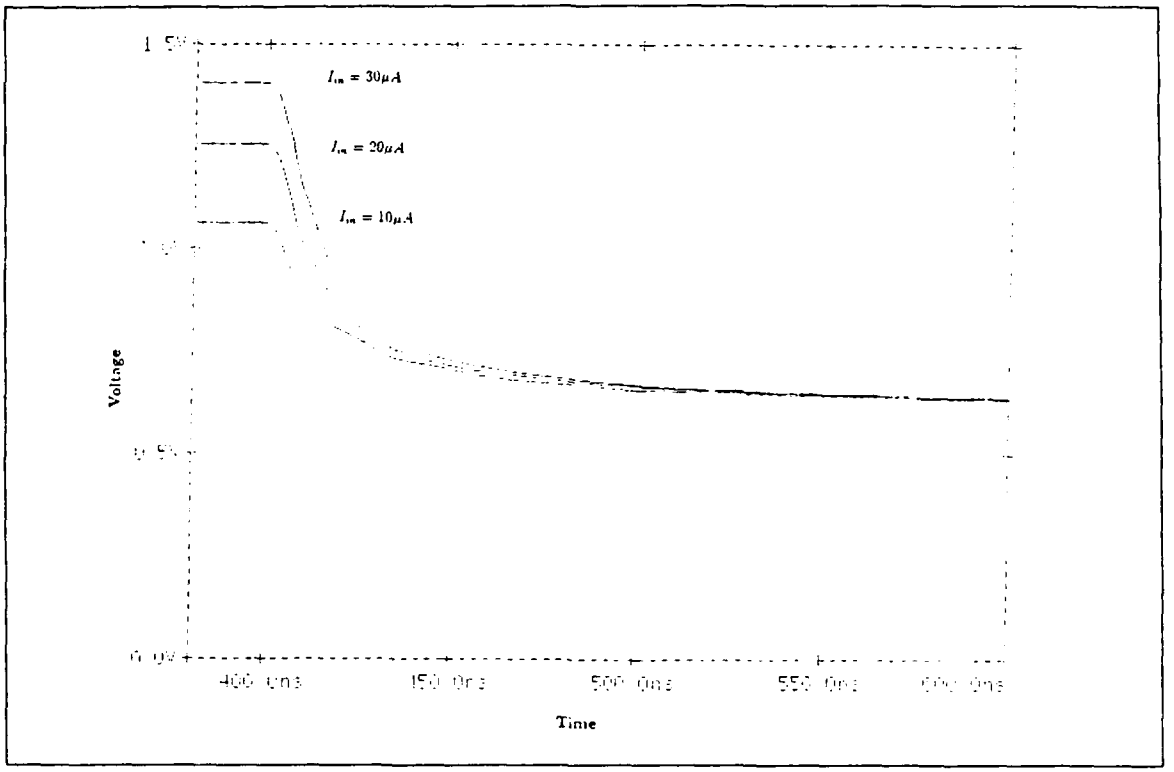


Figure 3.17: Vgs Developed Across Transistor M_1 (Step Up Inputs)

circuit of Fig. 3.13 were not successful. The only method found to improve the step-down characteristics of the latch was to increase the threshold current that defines the logic 0-to-1 transition point.

The final simulation for the device is a full-clocked operation on a slowly ramped input signal. As can be seen from Fig. 3.19, the output does in fact provide four distinct latch logic states. However, significant current spikes are produced at each clock transition, as well as during each logic state change. Although latch operation does not appear to be severely affected, these spikes remain a significant concern for the design.

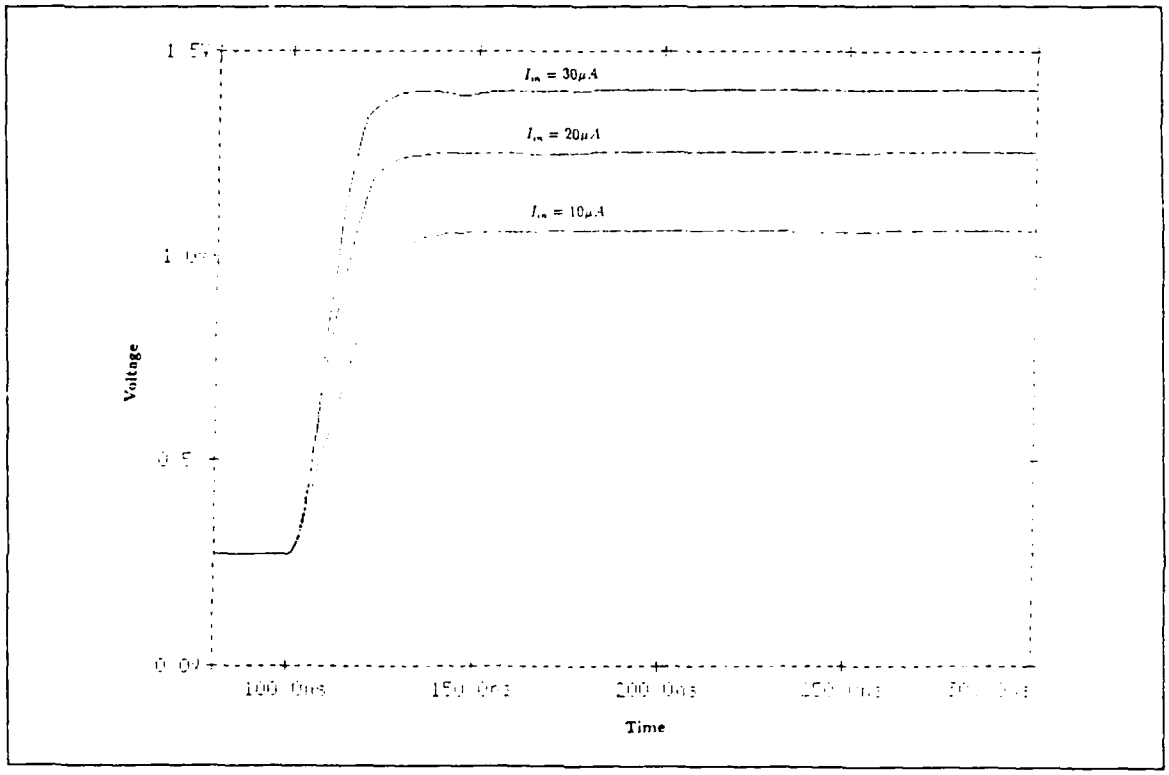


Figure 3.18: Vgs Developed Across Transistor M_7 (Step Down Inputs)

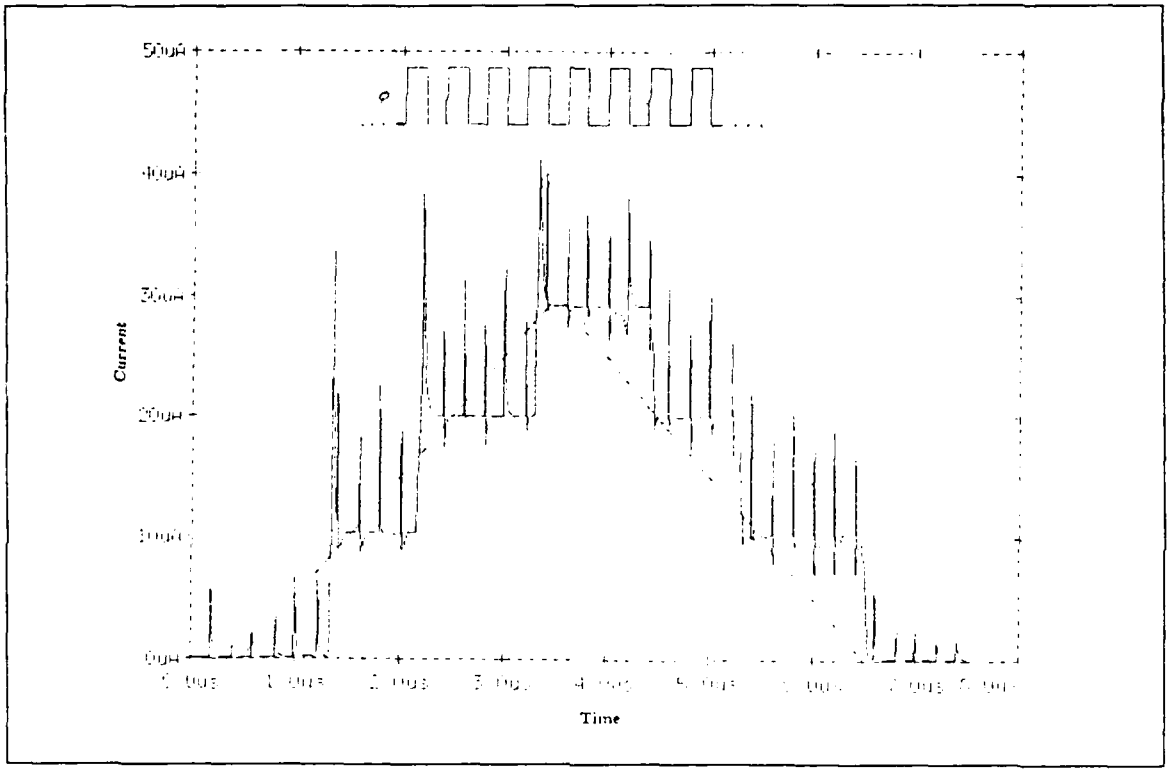


Figure 3.19: Clocked Operations

IV. MODIFIED CURRENT-MODE CMOS DESIGN

The complexity, speed, and power consumption of the four-valued latch described in the previous chapter inspired the examination of alternative designs.

A. CURRENT CONTROLLED INVERTERS

Fig. 3.5 shows that the comparator leg input/output characteristics of the four-valued latch are similar to those of a standard binary CMOS inverter. However, unlike an inverter, a constant reference voltage prevents the comparator's PMOS device from operating in cutoff and a path for current flow still exists when the comparator is in its logic low state. As a result, power will be dissipated even after I_{in} has exceeded the comparator's threshold. In an attempt to remove this contribution from the latch's already high static power requirements, each comparator leg was modified to perform the function of a current-controlled CMOS inverter, as shown in Fig. 4.1. As described below, however, there are several problems with this design.

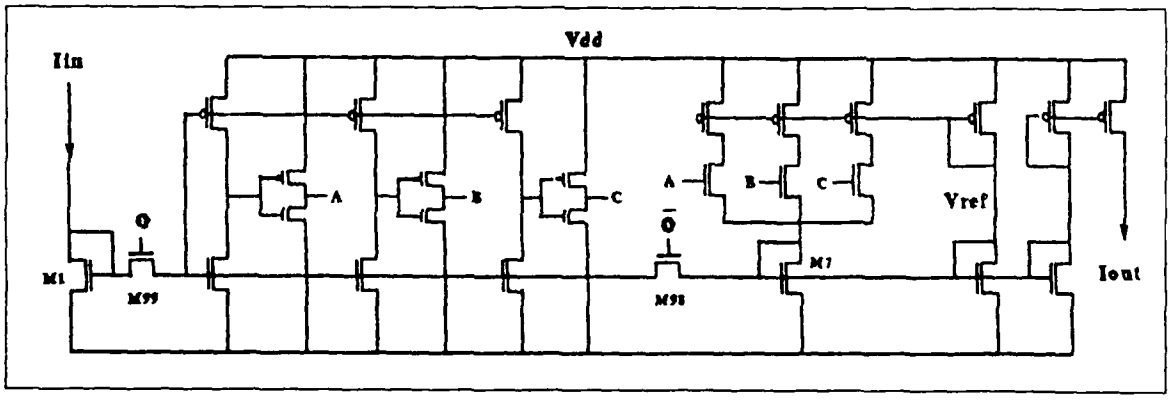


Figure 4.1: Modified Latch Using Current Controlled Inverters

First, with I_{in} limited to 30 μA and M_1 to minimum dimensions, the voltage developed across transistor M_1 is only Vgs_1 = 1.4 V. When the latch is in the setup mode, transistor M_{99} (in Fig. 4.1) will be biased on and Vgs_1 will be applied to the modified comparator network. Although Vgs_1 is sufficient for logic level discrimination, it is not high enough to force the comparator PMOS devices into cutoff as originally desired. In addition, as can be seen from Fig. 4.2, increasing the length of

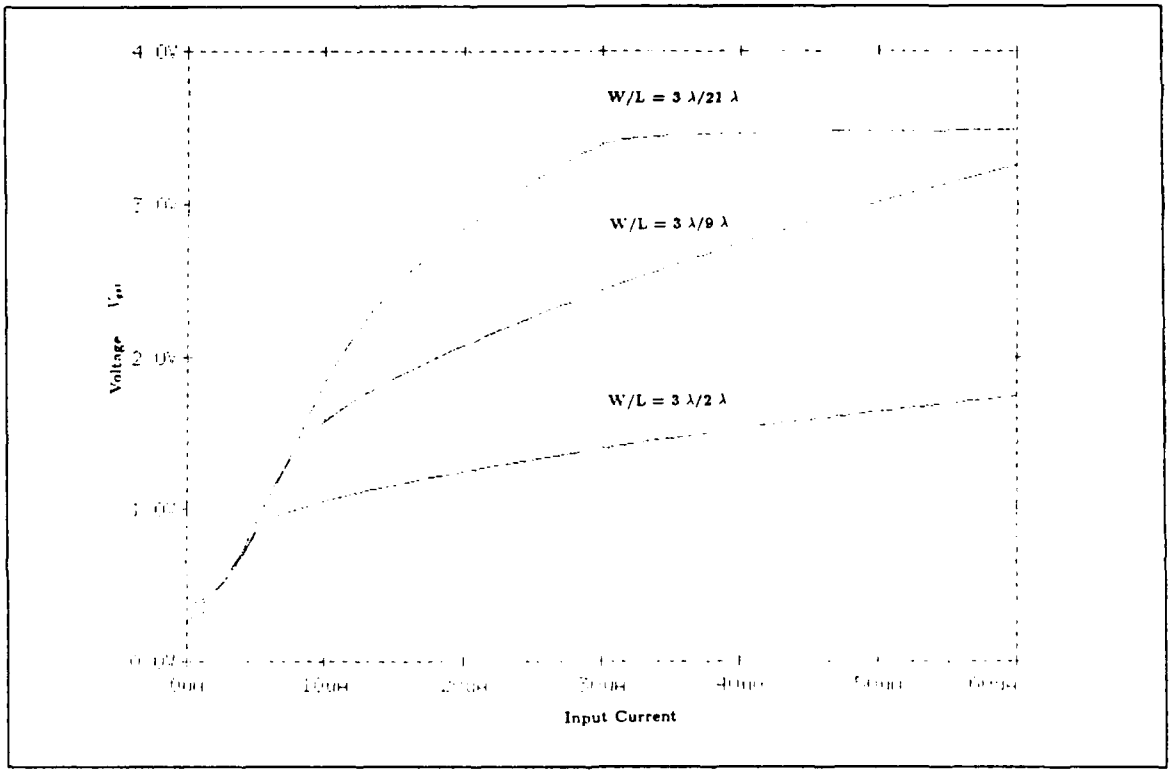


Figure 4.2: Vgs_1 as a Function of Iin

transistor M_1, (or the value of I_{in}), only provides a maximum Vgs_1 of approximately 3.5 V. With Vt_p = -0 84 V, Vdd = 5 V and $Vgs_1 \leq$ 3.5 V, $\mid Vgs_1 - Vt_p \mid$ will remain greater than 0 V and the PMOS devices will still not operate in cutoff.

To force the desired response, V_{dd} for the comparator subcircuit, (or Vt_p for the device), could be decreased. However, from

$$V_{sw} = \frac{V_{dd} + Vt_p + Vt_n\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}}, \tag{4.1}$$

the available range of comparator leg switching voltages also decrease and discrimination between input logic levels becomes extremely difficult to achieve.

Finally, although current flow exists in the previous design after I_{in} has exceeded the comparator's threshold, this current is limited to I_{th} by the comparator leg's active current source (see Chapter II.C.4). With the PMOS devices in the modified circuit unable to operate in cutoff, no method of limiting current flow exists for this design. As a result, static power requirements for this latch are significantly higher than that of Fig. 3.1, and was therefore discarded as a possible alternative to it.

Without a significant increase in circuit complexity, no method could be found to reduce comparator subcircuit static power requirements. In addition, to obtain logically restored output currents, reduced power designs for the encoder subcircuit could also not be found. Therefore, for current mode CMOS applications, the circuit of Fig. 3.1 appears to possess minimum static power requirements for the number of devices used.

B. DIRECT USE OF THE COMPARATOR OUTPUT VOLTAGES

In the original design, each comparator leg output voltage is complemented to form a binary control signal (see Fig. 3.4). Although the inverters provide sharp logic transitions, they increase latch delay time. In an attempt to regain this time, the NMOS pass transistors of the encoder subcircuit were replaced with PMOS devices and the comparator leg output voltages were used directly as the encoder control signals. As can be seen from Fig. 4.3, this allows six transistors to be removed from the design, significantly reducing circuit complexity.

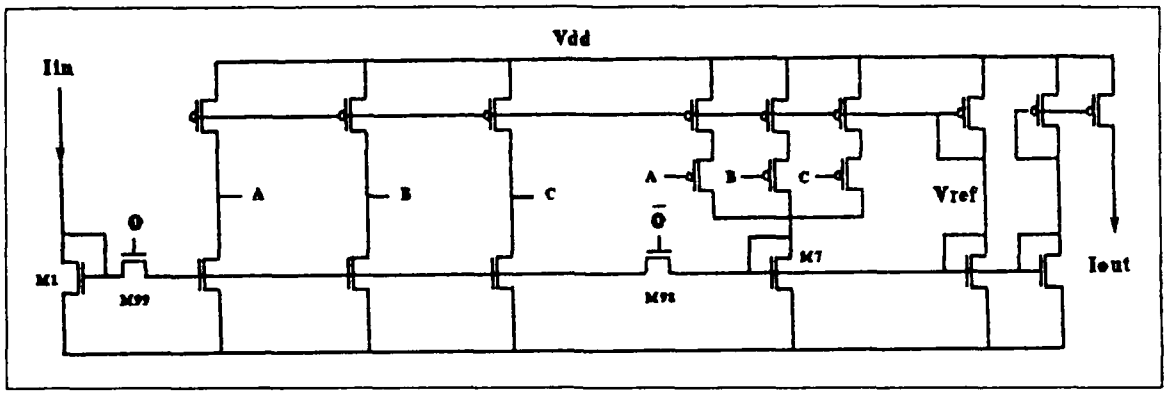


Figure 4.3: Modified Current-Mode CMOS Four-Valued Data Latch

At first glance, Fig. 4.4 may appear to provide disappointing PSPICE analysis. However, when the original input/output characteristics are superimposed onto these results, as is done in Fig. 4.5, this latch can be seen to possess several interesting properties. First, without the inverters, transitions from one logic state to another begin sooner than in the original design. This is as expected since comparator leg output voltages start transitioning as soon as I_{in} is applied to the latch (see Fig. 3.14). Also, since the control signals now change gradually, current spikes due to capacitive contributions of the latch output are minimized. Vestiges of current spikes can be seen in Fig 4.5, but they are significantly less that the circuit with inverters. Finally, as can be seen from Figures 4.6a, 4.6b and 4.6c, input step changes are also not accompanied by the severe current spikes experienced in the original design.

As can also be seen in Fig. 4.6, latch delay for step down transitions have been unexpectedly increased. Without sharp transitions from one logic state to another, the encoder's PMOS pass transistors have difficulty achieving cutoff operation. As a result, even though logic transitions start sooner than in the original design, they also last longer. For applications that cannot tolerate excessive current spikes, this design could be used as an alternative to the latch of Fig 3.1. It will not, however, improve its speed performance as originally desired. Since no other method could be

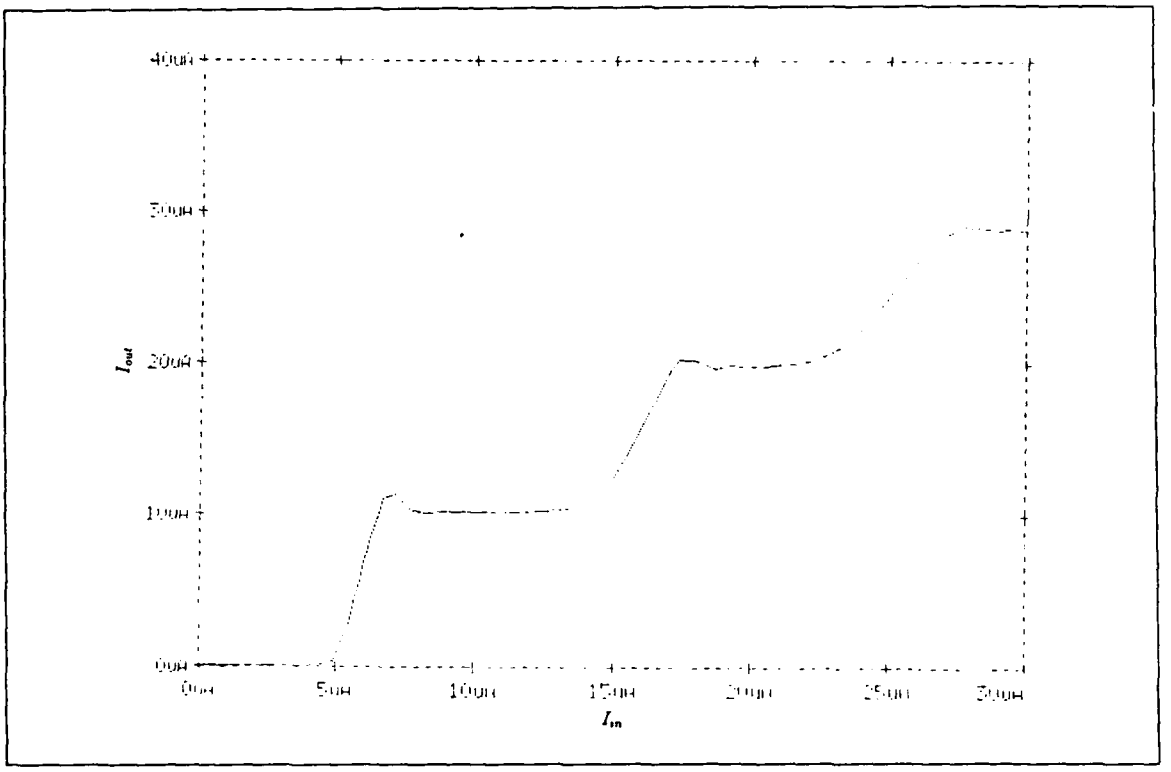


Figure 4.4: Modified Latch I/O Characteristics

found to simultaneously reduce circuit complexity and latch delay time, the circuit of Fig. 3.1 also appears to possess minimal characteristics for current-mode CMOS applications in this area as well.

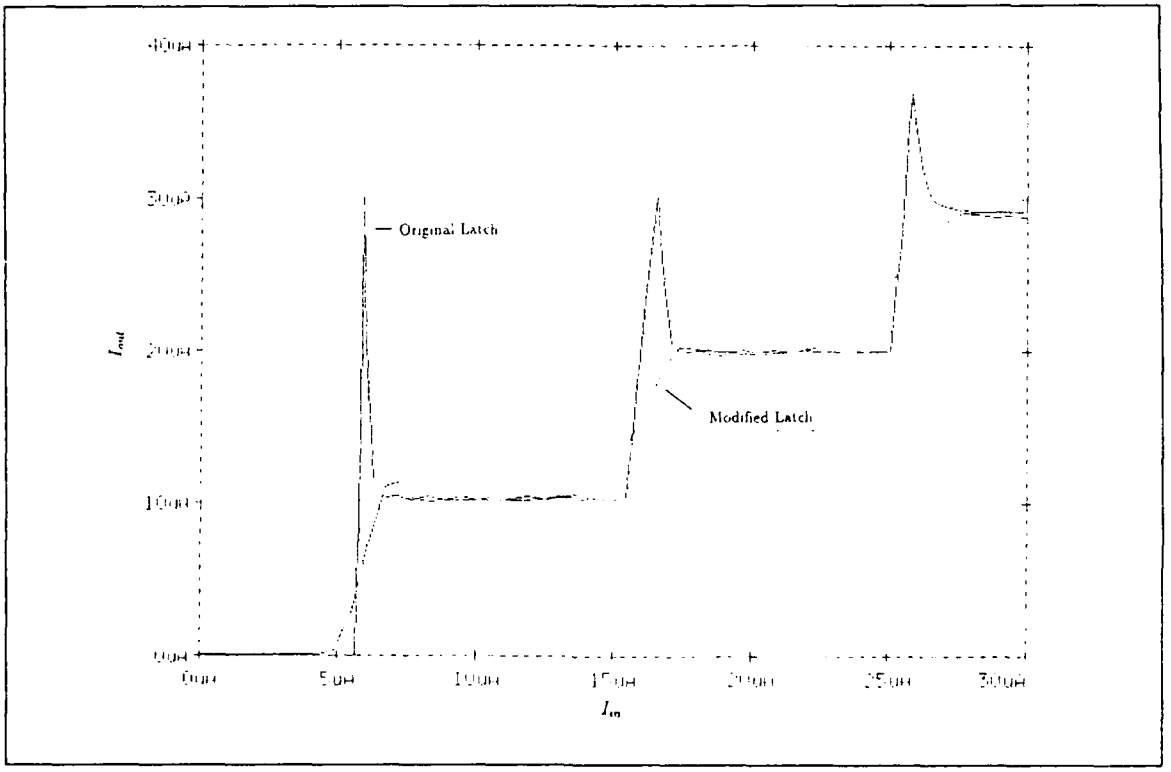


Figure 4.5: Comparison of Latch I/O Characteristics

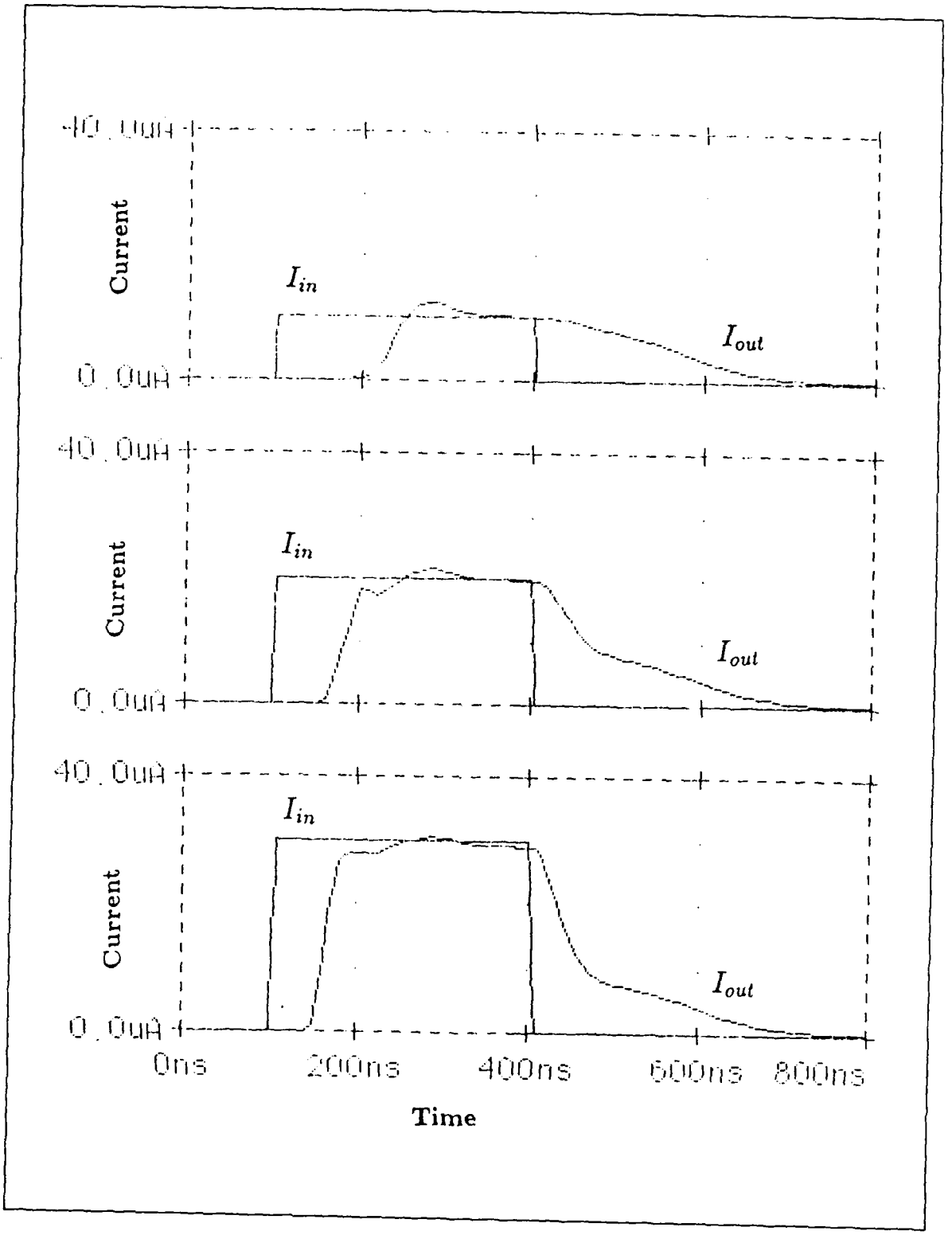


Figure 4.6: Modified Latch Response to Step Inputs

V. VOLTAGE-MODE CMOS DESIGNS

As shown in Chapter III, current-mode CMOS designs convert the latch input current into a voltage signal, which in turn causes a current to flow through the comparator network. The comparator network converts this current flow into three voltage control signals, which are then used by the encoder circuit to form the latch's final output current signal. This is an inefficient process and does not use the complementary device types available in CMOS technology for their intended purpose: power reduction. If a method could be found to remove the current to voltage conversions, then power requirements could be reduced, circuit speed increased and latch complexity minimized. That method is voltage-mode CMOS and is the topic of this chapter.

A. INPUT THRESHOLDING

With logic levels directly encoded as voltage, the necessity to convert between signal types is removed. Therefore, as shown in Fig. 5.1, standard CMOS inverters can be used to provide input logic level discrimination without the need for additional input circuitry. Since V_{in} is a four-valued logic signal, to distinguish the inverters of this circuit from their binary application, a unique switching voltage has been included in the schematic symbol of each device.

Recall from Chapter II that the inverter switching voltage (V_{sw}) can be obtained from

$$V_{sw} = \frac{V_{dd} + Vt_p + Vt_n\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}}. \tag{5.1}$$

With

$$\beta = K(W/L), \tag{5.2}$$

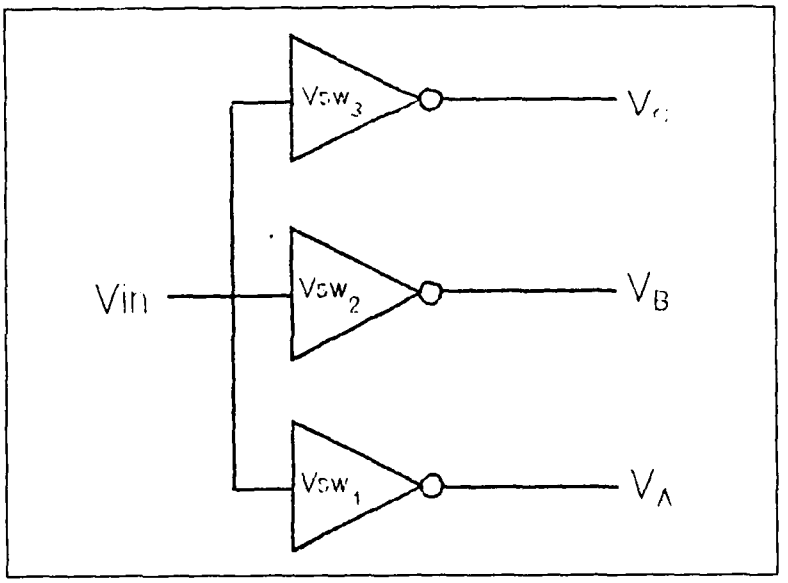


Figure 5.1: CMOS Inverters as Threshold Detectors

where $K = (\mu\epsilon/t_{ox})$ for the specific device type (see Fig. 5.2), a wide range of switching voltages may be obtained by simply adjusting the transistor geometries. For example, if $Vt_n = -Vt_p$, we have from Equation 5.1,

$$V_{sw} = \begin{cases} Vt_n & \text{for } \beta_n \gg \beta_p \\ V_{dd}/2 & \text{for } \beta_n = \beta_p \\ V_{dd} - \mid Vt_p \mid & \text{for } \beta_n \ll \beta_p \end{cases} . \tag{5.3}$$

Therefore, by selecting appropriate transistor width-to-length ratios, a distinct switching voltage can be established for each inverter. With V_{sw} set at the threshold voltage (V_{th}) between two logic levels, the inverters become threshold detectors and can be used to provide input logic level discrimination. As a result, the inverter output signals (labeled V_A, V_B and V_C in Fig. 5.1) provide three binary control signals as described in Table 5.1. The similarity between the current comparator outputs of Table 3.1 and the threshold detector outputs of Table 5.1 should be apparent. Although the necessity of converting between signal types (current $\leftrightarrow$ voltage) has been removed, as will be shown below, the necessity to convert from MVL to binary signals still exists.

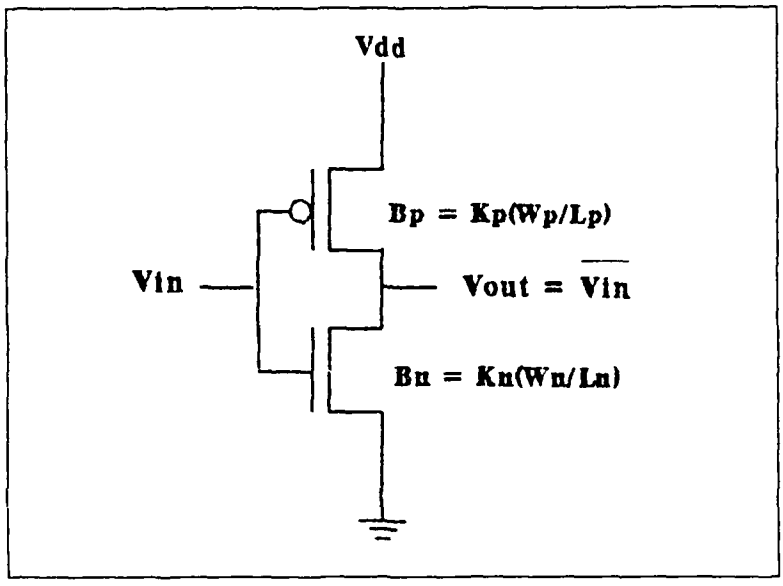


Figure 5.2: Standard CMOS Inverter

TABLE 5.1: THRESHOLD DETECTOR RESPONSE

Vin	V_A	V_B	V_C
Logic 0	HIGH	HIGH	HIGH
Logic 1	LOW	HIGH	HIGH
Logic 2	LOW	LOW	HIGH
Logic 3	LOW	LOW	LOW

B. VOLTAGE ENCODER

Unlike current, voltage signals cannot be arithmetically added at a common output node. Therefore, a method must be provided to ensure only one logic voltage level is present on the circuit output at a time. This is conceptually represented in Fig. 5.3, where the input voltage (V_{in}) controls which of the four intermediate logic signals will be presented to the circuit output (V_{out}). Since there are no four-valued transistors known to exist, the four-valued switch required in Fig. 5.3 must be constructed from binary devices. Therefore, MVL-to-binary conversions will be required for the input signal V_{in}. Using the circuit of the previous section to provide

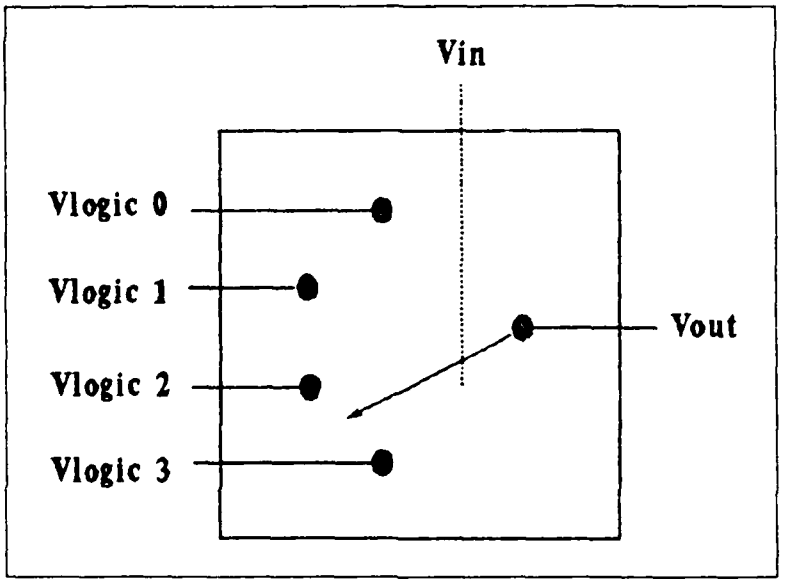


Figure 5.3: Voltage Encoder

the necessary binary control signals, Fig. 5.4 provides one method of realizing the four-valued voltage encoder circuit. With V_A, V_B and V_C obtained from Table 5.1 (and X's indicating "do not care" transistor states), circuit operation can be summarized as show in Table 5.2 below.

C. A 15 V CMOS DATA LATCH DESIGN

The four-valued data latch of Fig. 5.5 is constructed from the threshold detector and voltage encoder subcircuits described above. Since CMOS logic circuits can operate with a maximum supply voltage of up to 18 V [Ref. 19], 15 V was selected as V_{dd} for the initial design attempt. Although not convenient for VLSI applications, this value of V_{dd} provides separations between logic states that are equivalent to its binary counterpart, specifically 5 V.

With logic levels 0, 1, 2 and 3 defined as 0, 5, 10 and 15 V, respectively, threshold voltages were selected as 2.5, 7.5 and 12.5 V. To achieve these thresholds, Equation 5.1 provides a first approximation to the required transistor geometries; however, as noted

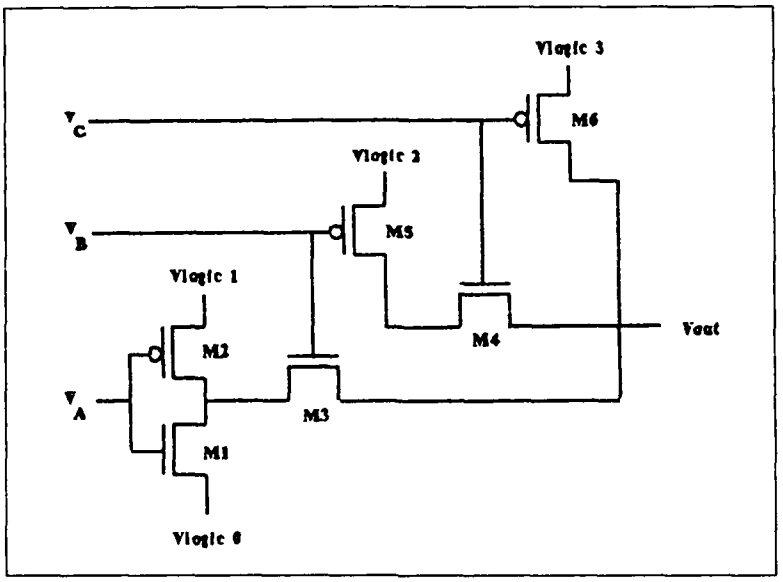


Figure 5.4: CMOS Realization of a Four-Valued Voltage Encoder

TABLE 5.2: ENCODER RESPONSE TO LOGICAL INPUTS

Input	Detector			Encoder Transistor States						Encoder
V_{in}	V_A	V_B	V_C	M_1	M_2	M_3	M_4	M_5	M_6	V_{out}
Logic 0	HI	HI	HI	ON	OFF	ON	X	OFF	OFF	Logic 0
Logic 1	LO	HI	HI	OFF	ON	ON	X	OFF	OFF	Logic 1
Logic 2	LO	LO	HI	X	X	OFF	ON	ON	OFF	Logic 2
Logic 3	LO	LO	LO	X	X	OFF	OFF	X	ON	Logic 3

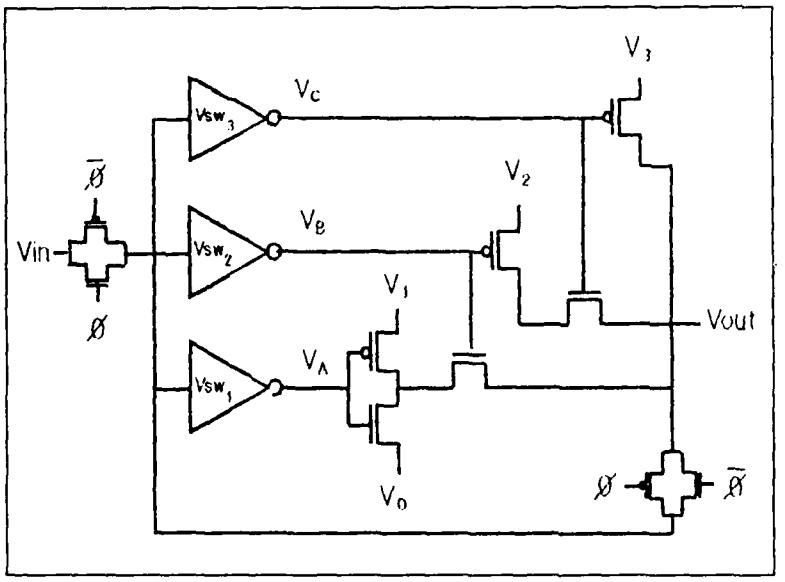


Figure 5.5: Four-Valued Voltage-Mode CMOS Data Latch

in Chapter III, PSPICE trial and error simulations are required to obtain the final width-to-length ratios.

As in the current-mode CMOS designs, this latch has two modes of operation, setup and hold. When the clock signal ϕ is a logic high, the latch operates in the setup mode. In this mode, V_{in} is accepted as the latch input, with Figures 5.6 and 5.7 providing the DC characteristics of the circuit. As can be seen from these figures, the desired threshold voltages have been achieved and well-defined logic states are displayed.

To determine propagation delay times, Figures 5.8a, 5.8b and 5.8c show circuit response to the logic transitions 0-1-0, 0-2-0 and 0-3-0 respectively. In performing these simulations, a clock skew of 4 ns per 5 V was used to approximate realistic rise and fall times. In addition, propagation delays are measured from the time V_{in} is increased, to the point where V_{out} exceeds the threshold voltage for the logic level to be achieved. As can be seen from Fig. 5.8, the worst case propagation delay of approximately 17 ns occurs for the logic 0-to-1 transition. Unlike the current-

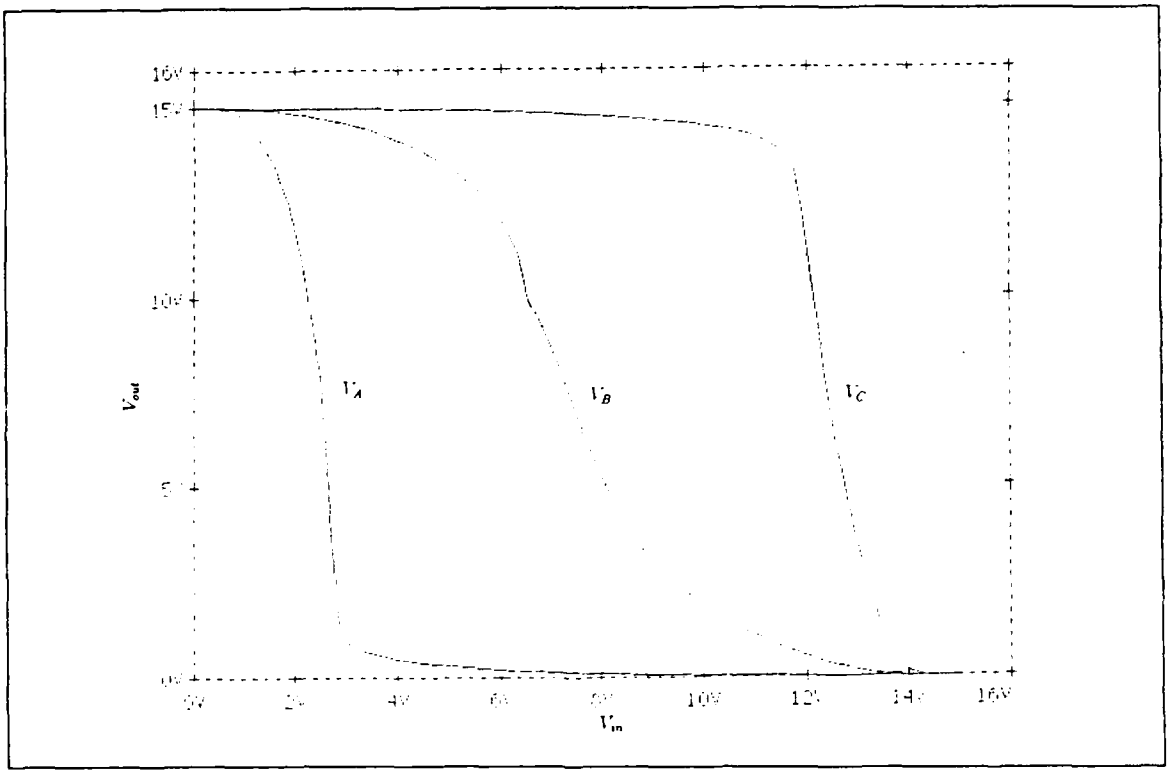


Figure 5.6: Threshold Detector DC Characteristics (Vdd = 15 V)

mode CMOS design, this latch does not "hang" at the logic 1 state during step-down transitions. Instead, the logic 3-to-0 state change provides the longest step-down delay of approximately 14 ns.

Clocked operations for a slowly ramped input voltage signal are shown in Fig. 5.9. As can be seen, minor voltage spikes are present at most clock transitions and are not of major concern. Voltage transients in excess of approximately 0.5 V, however, need further consideration.

The first two transients occur when the latch is in its logic 0 state. In both cases where these spikes occur, the clock is transitioning from a logic high to a logic low (i.e., the latch is transitioning from its setup to hold mode of operation). With a ramped input signal, the detector side of the feedback pass gate is at the voltage V_{in} (approximately 1.5 V), while the V_{out} side is at the ground potential (0 V). When

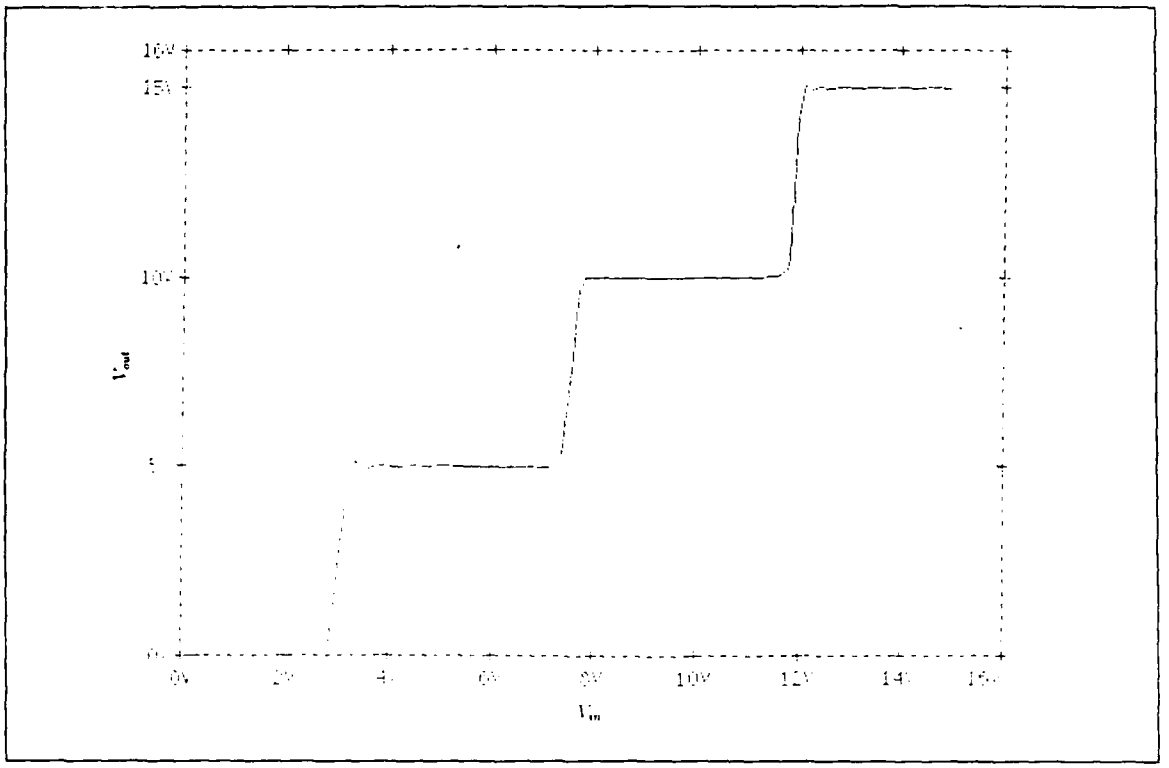


Figure 5.7: Latch Input/Output DC Characteristics (Vdd = 15 V)

the clock signal transitions from high to low, V_{in} is disconnected from the circuit, but parasitic capacitance on the threshold detector inputs require finite time for discharge. Therefore, when the feedback signal is connected to this line, V_{out} sees an almost instantaneous increase in voltage. With the original signal V_{in} relatively close to the logic 1 threshold, the threshold detector for that transition has already started to respond. Although its output is not yet low enough to allow the logic 1 power supply to be placed onto the circuit output, (i.e., a change of state to logic 1), it is restricting the path from V_{out} to the logic 0 power supply. Therefore, circuit response is delayed and the resulting voltage spike attains a peak value of approximately 0.8 V. This transient should not effect latch operations.

A similar situation occurs when the latch is in its logic 3 state. In this case, however, V_{in} is lower than V_{out} and with V_{in} at approximately 14 V, the PMOS device

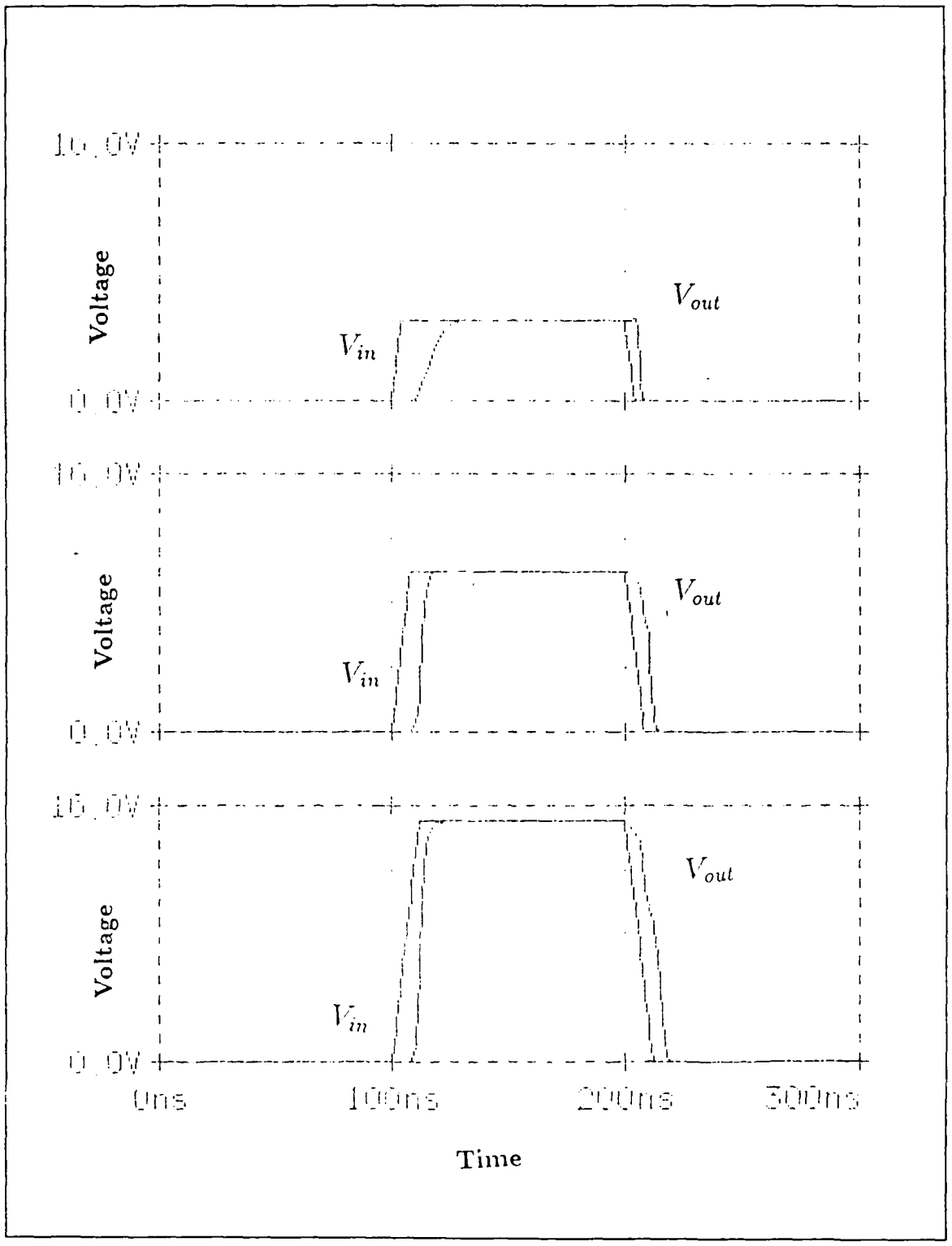


Figure 5.8: Latch Response to Step Inputs (Vdd = 15 V)

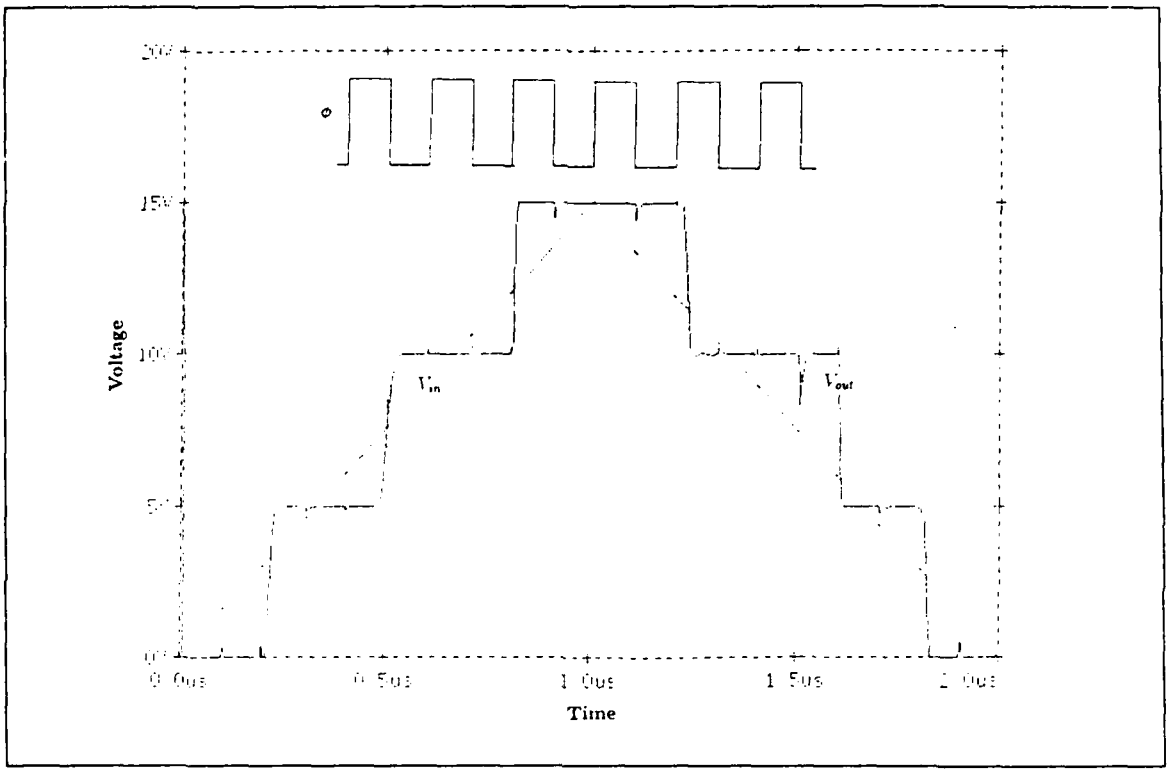


Figure 5.9: Clocked Operations (Vdd = 15 V)

for the logic 2/3 threshold detector has not yet achieved cutoff operation. As a result, a voltage slightly greater than ground potential will be applied to the PMOS pass transistor M_9 (see Fig. 5.5). From the current-mode CMOS chapters, PMOS devices with gate voltages greater than 0 V can be considered as current sources, where I_{out} decreases as the transistor's gate voltage is increased. When the clock transitions from high to low, the feedback pass gate connects the threshold detector inputs to the V_{out} line, which causes transistor M_9 to see an almost instantaneous increase in load. Since it cannot respond instantaneously, a downward voltage spike occurs. These transients achieve peak values of approximately 0.7 V and should also not affect clocked operations for this device.

The largest voltage transient occurs when the latch is in its logic 2 state (with V_{in} decreasing) and does not appear to have a symmetric counterpart as seen for the

other examples. However, this should not be totally unexpected. When the voltage spike occurs, V_{in} is almost at the threshold (7.5 V) for the logic 2-to-1 transition. If we examine the case where V_{in} is increasing toward this value (at approximately 0.5 μs in Fig. 5.9), we see the threshold is achieved just after the latch has entered the setup mode and the transition from a logic 1 to a logic 2 occurs as expected. However, as V_{in} decreases toward this value, the logic 2-to-1 threshold voltage is achieved while the latch is transitioning from its setup to hold mode of operation. Since propagation delays are experienced for any logic transition (see Figures 5.8a, 5.8b and 5.8c), V_{out} does not respond quickly enough for the feedback signal to fall below 7.5 V. As a result, the latch restores its original logic 2 value and must wait until the next clock cycle to make the final logic 2-to-1 transition. This indicates that the latch is operating properly, but shows adequate setup and hold times must be provided to obtain predictable latch outputs.

D. A 5 VOLT CMOS DATA LATCH

As noted in the previous section, a V_{dd} of 15 V is inconvenient for VLSI applications. Although PSPICE simulations show favorable results for this design, circuit supply voltages need to be reduced. As a result, the design of Fig. 5.5 was modified to accommodate V_{dd}= 5 V. Since the circuit layout for this design is identical to that of Fig. 5.5, it has not been reproduced here. However, device geometries significantly differ from those of the previous design and have been included in Appendix B for reference.

For the initial design attempt, equally spaced logic levels of 1.66 V were selected. With logic levels 0, 1, 2 and 3 defined as 0, 1.66, 3.33 and 5.0 V respectively, threshold voltages were selected at 0.8, 2.5 and 4.16 volts. However, these selections present several immediate problems. First, the threshold voltage between logic 2 and 3 is

identically equal to $V_{dd} - |Vt_p|$. From Equation 5.1, this can only be achieved when $\beta_p = \infty$. Therefore, this threshold had to be lowered to approximately 3.8 V to obtain reasonably-sized transistor geometries (see Appendix B). In addition, to provide equally spaced transitions for both the logic 1 and logic 2 states, this also required lowering the 2.5 V threshold to approximately 2.38 V.

Next, with intermediate voltage power supply V_{logic1} at 1.66 V, propagation delay associated with the logic 0-to-1 transition becomes entirely unacceptable. Figure 5.10 shows the effect of lowering V_{logic1} when a slowly ramped input voltage is

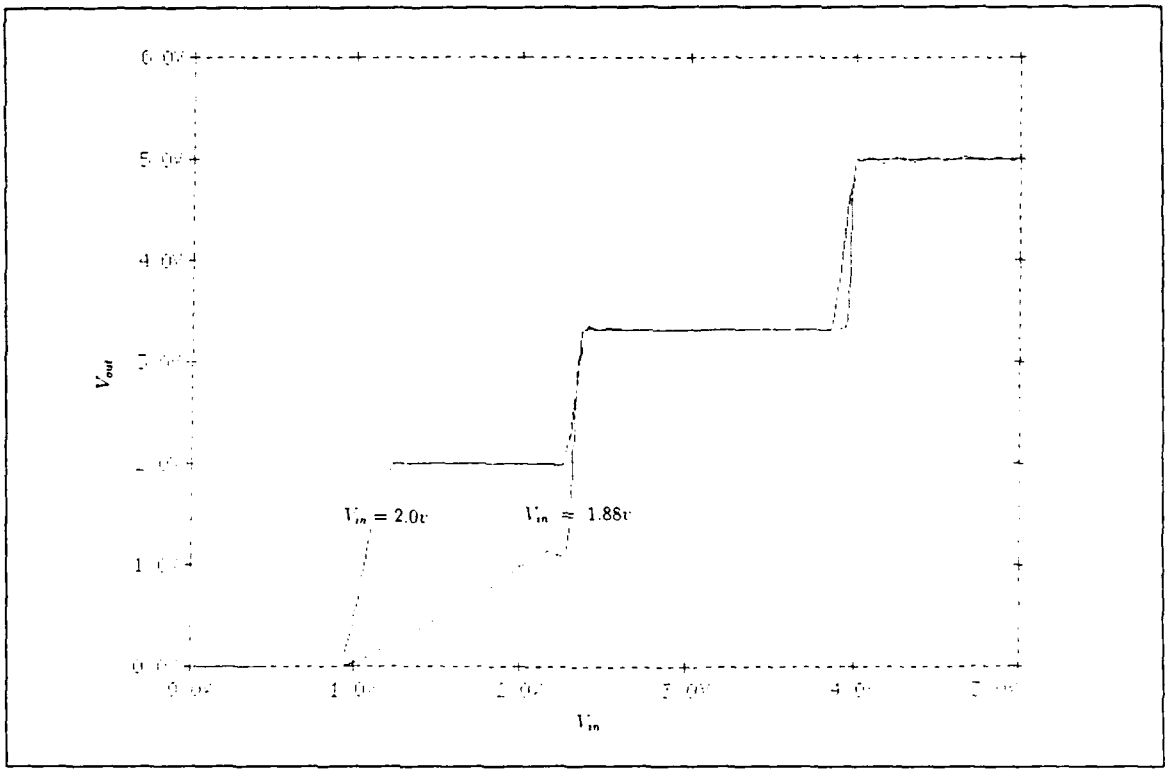


Figure 5.10: Latch Output as a Function of V_{logic1}

applied to the circuit. As can be seen, with V_{logic1} below approximately 1.88 V, the delay between logic 0 and logic 1 is so excessive that the logic 1 state is never actually achieved. Recall that the threshold voltage for this transition was selected at 0.8 V. Since this value is close to Vt_n (unlike the 15 V model), transistor geometries required

to achieve this threshold are large. This increases device capacitance, and therefore delay times. Since the logic 1 state cannot be entered until transistor M_7 operates outside the cutoff region (see Fig. 5.5), the longer it takes for the threshold detector to provide $V_A \leq V_{logic1}$, the longer the device will take to transition from logic 0 to 1. From PSPICE trial and error simulations, a voltage V_{logic1} of 2.0 volts provides satisfactory operation and the logic 0-to-1 threshold was maintained at 0.8 V.

With these modifications made, DC characteristics, as shown by Figures 5.11 and 5.12, are favorable. However, with higher device geometries required for both the

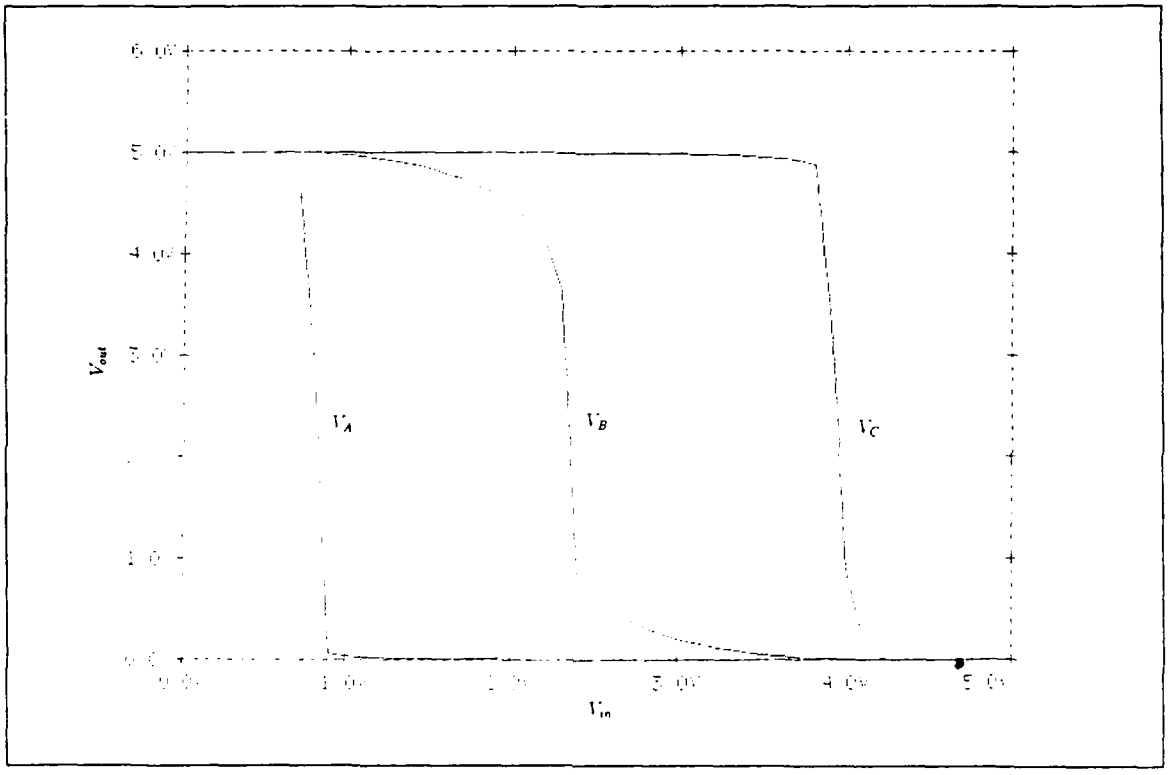


Figure 5.11: Threshold Detector DC Characteristics (Vdd = 5 V)

logic 1-to-2 and 2-to-3 threshold detectors, parasitic capacitance will be high. This leads to slower response times, and transient analysis can be expected to perform worse than the 15 V model. (These effects are not included in the PSPICE DC transfer curves of Figures 5.11 and 5.12).

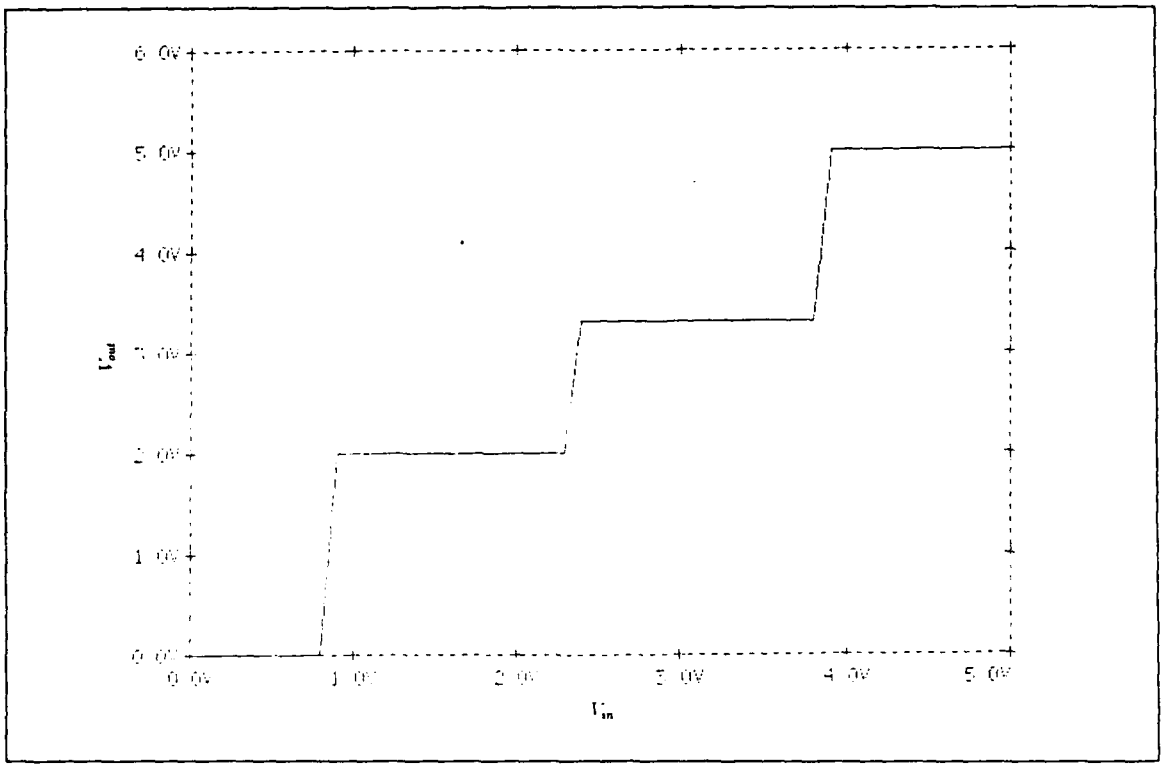


Figure 5.12: Latch Input/Output DC Characteristics (Vdd = 5 V)

To show this effect, Figures 5.13a, 5.13b and 5.13c provide latch response to the logic transitions 0-1-0, 0-2-0 and 0-3-0, respectively, with delay times for each design summarized in Table 5.3. As can be seen from Table 5.3, delay times for this latch are significantly longer than for the 15 V model. From these simulations, worst case propagation delays occur for the logic 0-3 transition and require approximately 55 ns to exceed the logic 3 threshold. This latch differs from the previous designs in that the worst case delays do not occur for the logic 0-to-1 transition. As can be seen from Figures 5.13b and 5.13c , each individual logic state change is specifically identifiable as the latch progresses to its final logic 3 state. This adds delay at the passing of each logic level and is a direct result of the increased role that parasitic capacitance plays in this circuit.

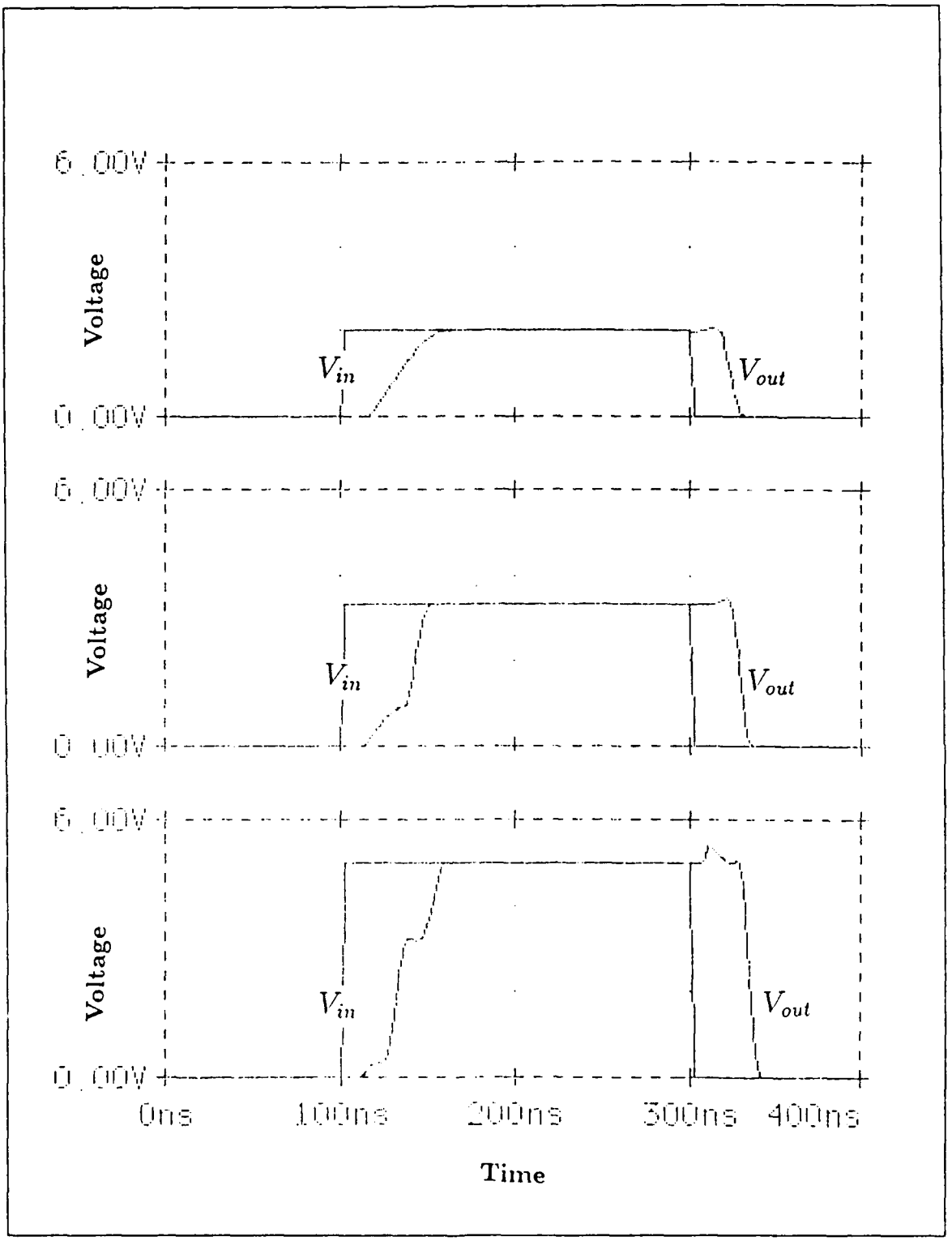


Figure 5.13: Latch Response to Step Inputs (Vdd = 5 V)

TABLE 5.3: COMPARISON OF VOLTAGE-MODE DELAY TIMES

Logical Step Input	V_{dd} = 15 V Data Latch Propagation Delays	V_{dd} = 5 V Data Latch Propagations Delays
0 - 1	17 ns	55 ns
0 - 2	14 ns	45 ns
0 - 3	13 ns	40 ns
3 - 0	14 ns	38 ns
2 - 0	11 ns	30 ns
1 - 0	6 ns	25 ns

Another effect produced by increased parasitic capacitance can be seen in Fig. 5.14. For the same clock frequency and rate of the ramped input signal V_{in}, Fig. 5.14 becomes a scaled version of Fig. 5.9. When these two figures are compared, the same output voltage transients can be seen to occur; however, increased delay times for the 5 V design exaggerate their effect. Although four distinct logic states are preserved, this latch will perform much less satisfactorily when the input logic signals are not close to the predefined logic states of the device. It should be noted that ramped input signals are rare in digital systems; however, this signal type provides insight to latch operations in the presence of noise. As can be seen from Fig. 5.14, provided noise levels do not exceed threshold voltages, this device will retain its logic state.

E. INTERMEDIATE VOLTAGE GENERATION

The voltage-mode design of Fig. 5.5 requires additional inter-device connections to provide the supply voltages V_{logic1} and V_{logic2}. This is undesirable and can be avoided by using dioded-connected transistors in a voltage-divider network. Many such networks are possible, however, for simplicity, the circuit of Fig. 5.15 was selected. In addition, since a 15 V data latch will be difficult to implement in VLSI, only the 5 V design of the previous section will be considered.

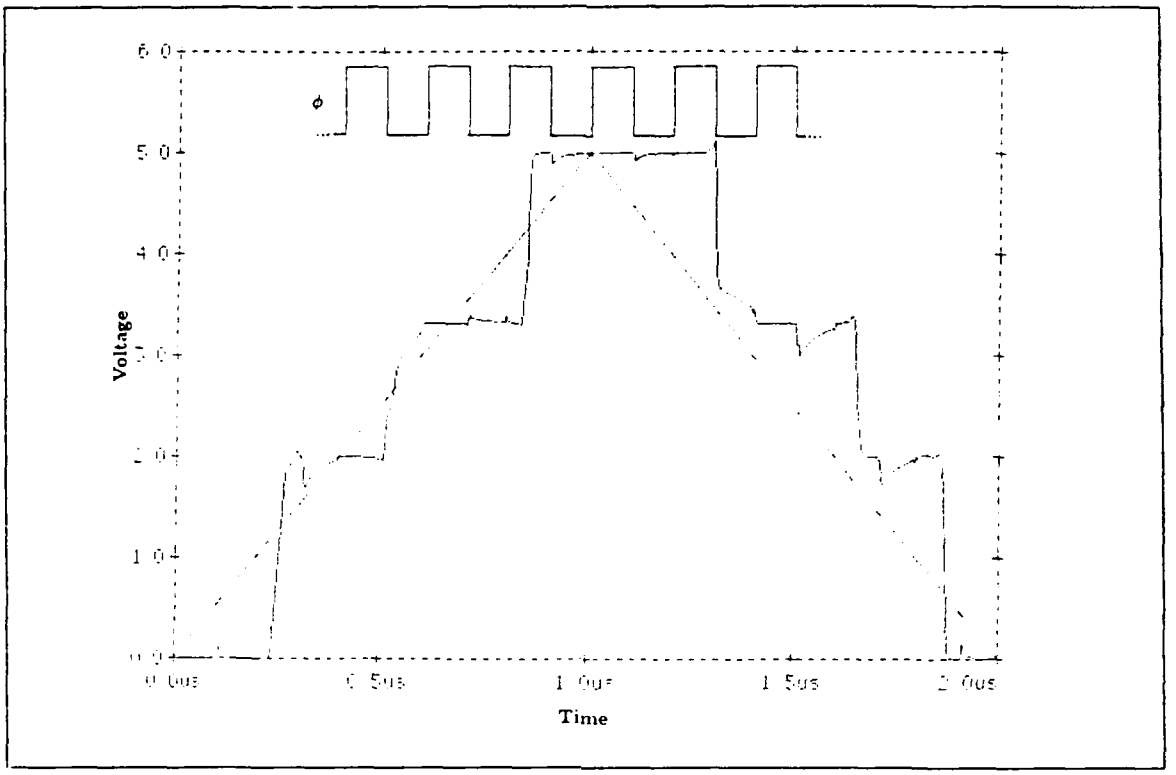


Figure 5.14: Clocked Operations (Vdd = 5 V)

A first approximation for the device geometries of Fig. 5.15 was obtained from Equation 2.8. PSPICE trial and error simulations provided final dimensions (see Appendix B) and, at a 10 μA average current flow, V_{logic1} and V_{logic2} were set at 2.01 and 3.37 V respectively.

The final circuit layout is shown in Fig. 5.16, with favorable DC characteristics show in Fig. 5.17. With the addition of the voltage-divider network, a small propagation delay is introduced whenever the intermediate voltages are called upon to provide V_{out}. This can be seen from Figures 5.18a, 5.18b and 5.18c, where approximately 10 ns have been added to the logic 0-1 and 0-2 transitions. Clocked operations are also effected, and as can be seen from Fig. 5.19, output voltage transients are further exaggerated in the logic 1 and logic 2 storage states of the device. However, these transients still only achieve a magnitude of approximately 0.4 V and do not result

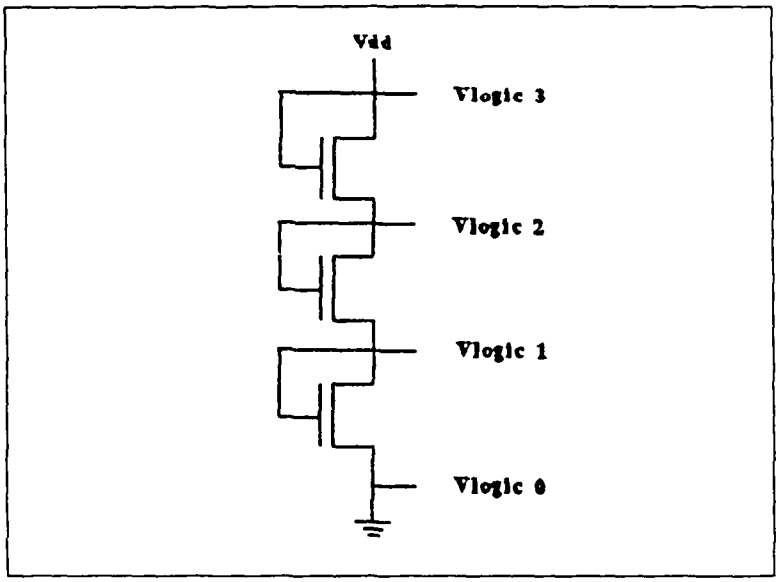


Figure 5.15: Voltage-Divider Network

in a loss of logic state. Therefore, as long as the input voltage signal is close to the predefined storage states of the device, the latch should perform satisfactorily.

This is the first known design attempt of a voltage-mode CMOS four-valued data latch. As such, the fact that it is capable of maintaining its logic state in the presence of adverse signals is highly encouraging.

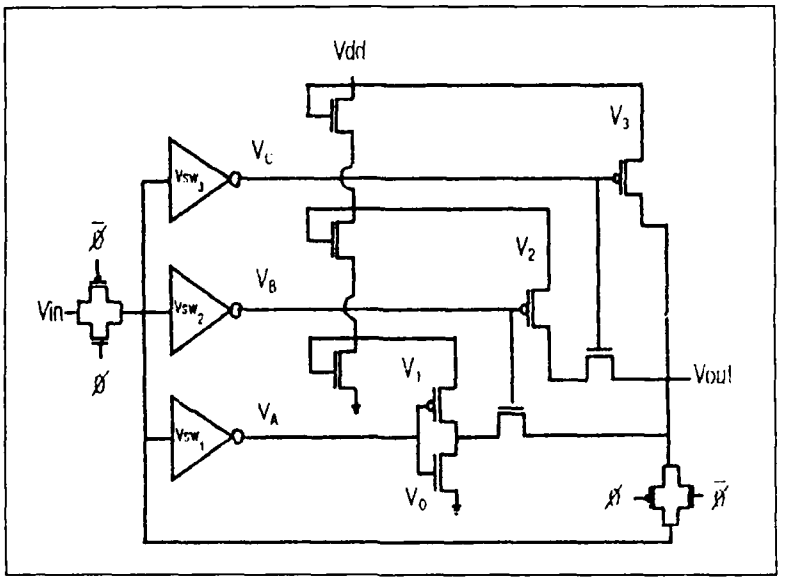


Figure 5.16: Modified Voltage-Mode Four-Valued Data Latch

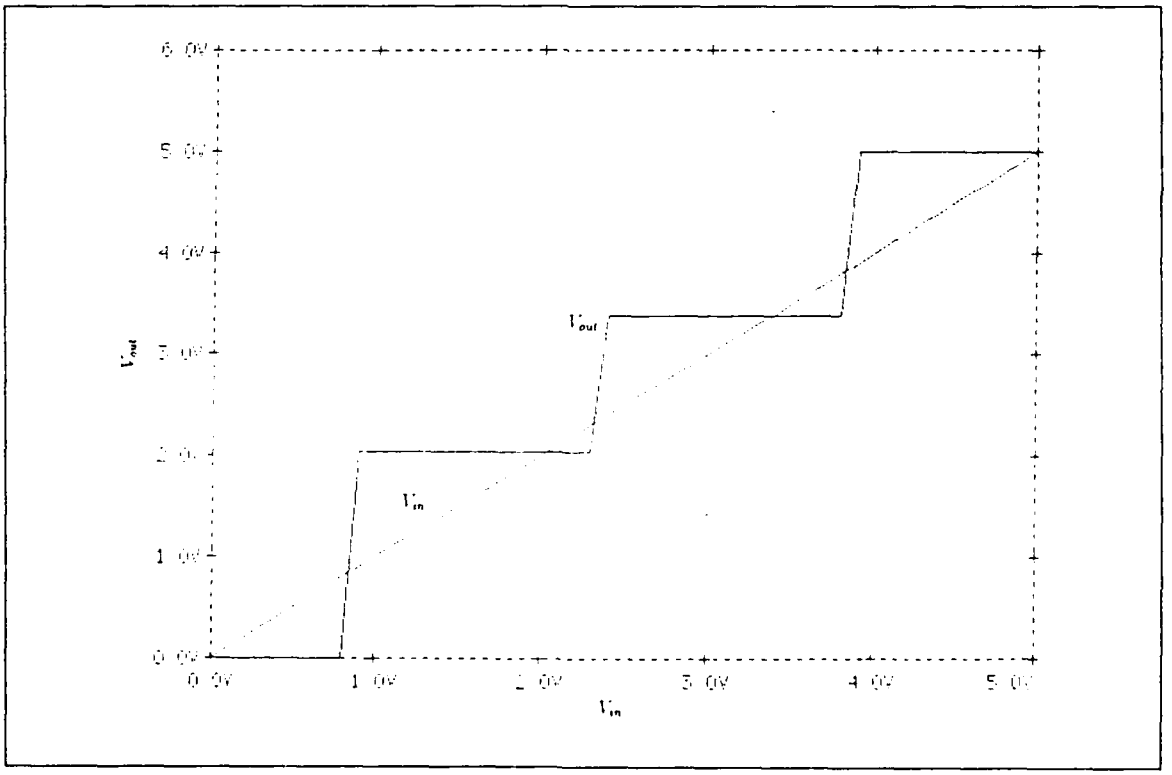


Figure 5.17: Modified Latch Input/Output DC Characteristics

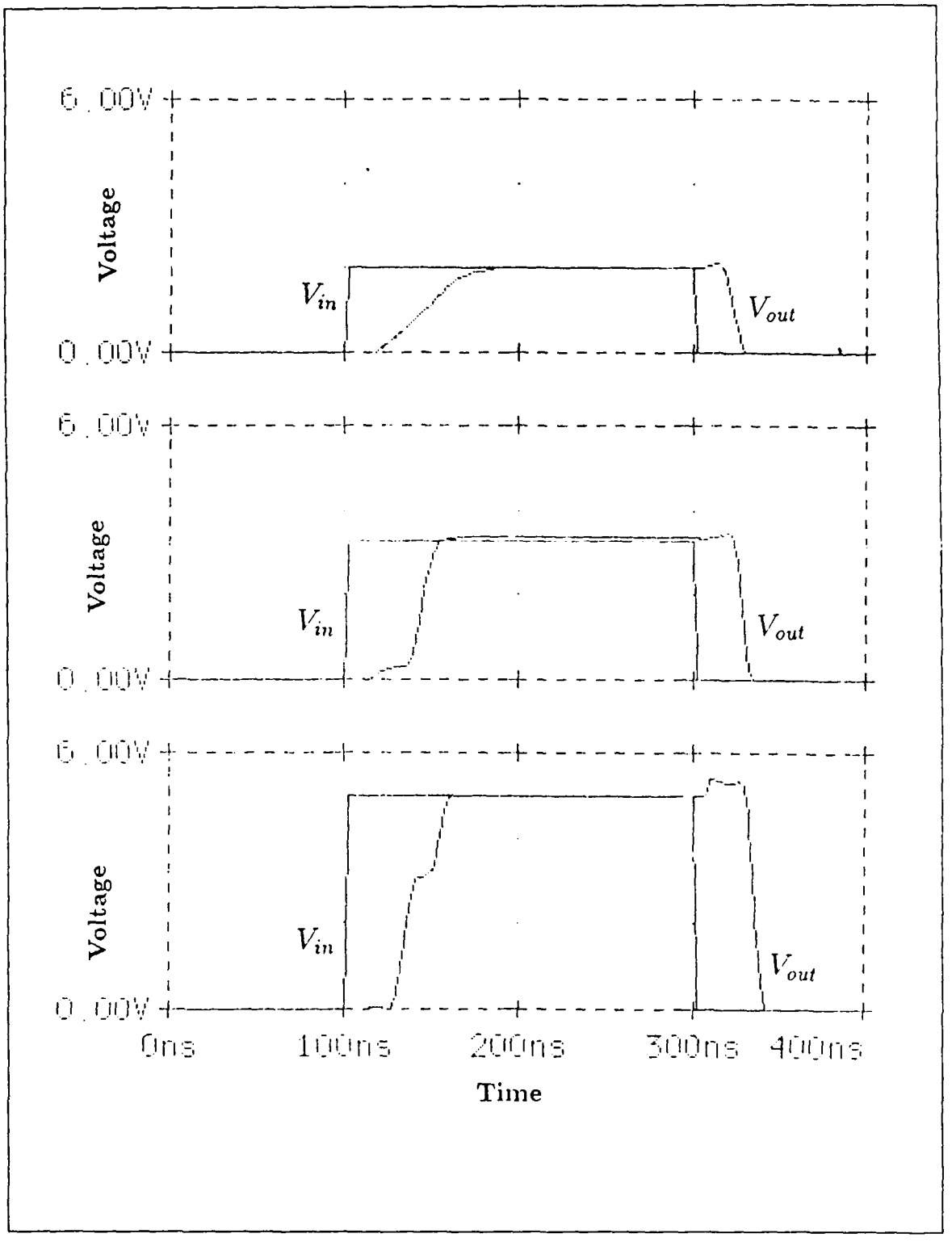


Figure 5.18: Modified Latch Response to Step Inputs

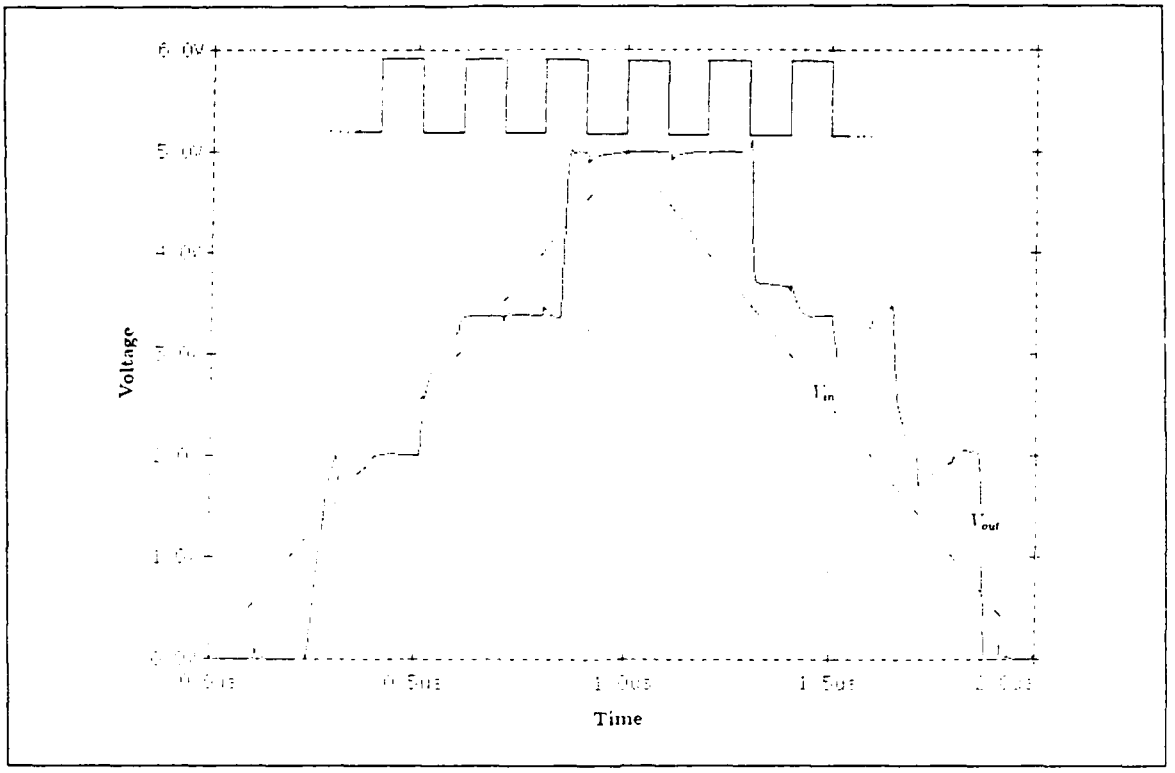


Figure 5.19: Modified Latch Clocked Operations

VI. COMPARISONS BETWEEN DESIGNS

Each of the designs presented in the previous chapters have merits, as well as problems. This chapter highlights the advantages and disadvantages of each device and describes applications where they may be used.

A. STATIC POWER REQUIREMENTS

Three of the five MVL data latches presented in this study require the use of a voltage-divider network. For the current-mode CMOS designs, a voltage less than V_{dd} is needed to perform input thresholding operations, as well as to provide logically restored output signals. For the voltage-mode CMOS designs, logical output signals are not possible unless intermediate voltages are either provided to or generated by the latch. In each case where voltage divider networks are used, static power will be dissipated, regardless of the logical state being stored.

As can be seen from Fig. 3.1, the reference voltage of a current-mode CMOS device is never directly connected to the circuit output. Therefore, a relatively constant capacitive load is presented to the voltage divider network of this circuit. For voltage-mode designs, the intermediate power supplies (V_{logic1}, V_{logic2}) are specifically required to provide the latch output. They must therefore be capable of providing that output in the presence of changing loads. As a result, lower currents can be used for the divider network of current-mode CMOS designs than for their voltage-mode counterpart. As an example, the first current-mode CMOS design required approximately 8.7 μA to develop the latch's reference voltage. This results in a static power consumption of approximately 43 μW. In contrast, 10 μA was found to be the minimum current flow for the voltage divider network of Fig. 5.17. Since V_{dd}=5 V

for this design, 50 μW are required. In addition, although a 10 μA current flow was found to be satisfactory for the voltage-mode latch simulations of this study, it is unlikely this will be sufficient to supply low input impedance logic devices. In this case, increased current flow through the divider network will be required in order to supply the higher demand loads with adequate logic inputs. Therefore, the 50 μW of static power required for this voltage divider is only achievable in applications where the latch output is to be connected to high input impedance devices.

When the latch operates above the logic 0 state, the 5 V voltage-mode CMOS designs have the advantage. With threshold detectors constructed from standard CMOS inverters, an input logic 0 or 3 will force one of the transistors in each detector to operate in cutoff. For these logic states, static power requirements are limited to the voltage-divider network. However, unlike binary inverter applications, intermediate input voltages may also represent stable latch storage states. For these states (logic 1 or logic 2), threshold detector outputs will transition from high to low but the input voltage will be insufficient to force their PMOS devices into cutoff. As a result, current will flow through the threshold detectors during intermediate latch storage states. From PSPICE simulations, 38 and 24 μA were observed as the average current flow through these devices for the logic 1 and logic 2 storage states respectively. Overall static power consumption for this latch is summarized in Table 6.1.

For the current-mode CMOS designs, static power consumption increases with the storage state of the device. At logic 0, power consumption is limited to establishing a reference voltage. However, for logic levels greater than logic 0, static power contributions are provided by: 1) each output connected current source of the encoder network, 2) all three comparator leg current sources; and, 3) both the input and output current mirrors. As an example, for a logic 2 storage state, an input current of 20 μA develops approximately 1.2 V across the NMOS transistors of the

input and output current mirrors. This dissipates approximately 48 μW. The three legs of the comparator network will pass 5, 15 and 20 μA from V_{dd} to ground respectively. This dissipates approximately 200 μW. Finally, two encoder current sources are connected to the summing junction and requires 20 μA x 5 V = 100 μW. When the voltage-divider network is included, this results in a total of approximately 391 μW. Power consumption for the remaining logic levels of this latch are also summarized in Table 6.1.

TABLE 6.1: STATIC POWER CONSUMPTION

Logic State	Current-Mode (V_{ref} = 2.51 V)	Voltage-Mode (V_{dd} = 5 V)
0	43 μW	50 μW
1	234 μW	240 μW
2	391 μW	170 μW
3	497 μW	50 μW
AVG	291 μW	128 μW

If V_{dd} for the voltage-mode device is increased to 15 V, static power requirements become a limiting consideration for this design. For this latch, even if intermediate voltage levels are provided externally, (i.e., no logic 0 or 3 static power consumption), the logic 1 and 2 storage states dissipate approximately 14 and 19 mW themselves. Therefore, although LSI and MSI technology will allow V_{dd}=15 V [Ref. 19], this latch can only be used where static power is not a concern for the design. As such, its applications are severely limited.

B. SPEED

For the MVL storage devices of the study, decreased delay time appears to be accompanied by either increased static power consumption or decreased stability of

the output signal. As an example, one method to improve the speed performance of the current-mode CMOS design is with the addition of cascode-connected current sources and 5 μA biasing currents [Ref. 17]. However, a significant increase in circuit complexity is required and additional static power is consumed. For applications that can tolerate the additional power consumption (and additional chip area), this device is superior to any of the simplified current-mode CMOS models examined by this study. As a specific example, the concept of Fig. 3.1 was used to provide a transparent latch capability to a four-valued full adder by K. W. Current in Ref. 20. Although direct comparisons cannot be made with the latch of Fig. 3.1, worst case setup and hold times of approximately 35 ns for single logic transitions were experimentally obtained. This is significantly faster than the simulation results of Fig. 3.16.

In the voltage-mode CMOS devices, hold times start at approximately 55 ns (for V_{dd}=5 V) and can be increased to about 20 ns only at great expense in the area of power consumption. Although the 5 V model consumes less power and requires less chip area to implement than the current-mode designs, its output is significantly less stable. Here again, additional power consumption is required to increase latch output stability.

C. CIRCUIT COMPLEXITY

In its most simplified form, the current-mode CMOS data latch requires 27 transistors in three major subcircuits to perform its task (see Fig. 3.1). When cascode current sources and input biasing currents are added to the design [Ref. 17], circuit complexity grows even larger. In contrast, voltage-mode designs only require 16 transistors; 19 if intermediate voltages are provided internally. Although a simple device count is an incomplete comparison, it does provide a measure of the circuit

complexity, as well as the chip area required for its implementation. Therefore, voltage-mode CMOS designs have a significant advantage in this area.

Although not obvious from a circuit schematic point of view, another area where current-mode CMOS designs increase circuit complexity is with signal conversion. As noted in Chapter V, each of the three subcircuits in Fig. 3.1 convert current to voltage or voltage to current. This is inefficient and tends to negate the low power capabilities available to CMOS technology. In addition, tracing the input signal to the latch output becomes a difficult task and results in a heavy reliance on trial and error simulations to obtain the desired circuit response. This requires a more intensive design effort than is needed for voltage-mode devices.

As can be seen, voltage-mode CMOS devices are capable of storing multiple-valued input signals for less power, comparable speed and reduced circuit complexity. Although many problems remain to be solved, with the potential advantages that stand to be gained, these devices are deserving of additional future studies.

VII. MVL VS. BINARY

One of the most difficult problems that must be overcome in the design of a multiple-valued data latch is logic level restoration. Unlike binary, a simple method for restoring logic does not exist. Instead, each multiple-valued input must first be converted to reliable binary signals, with those signals then used to form the restored circuit output. This is a direct result of device technology, where transistors capable of switching between more than two logic states have not yet been developed [Ref. 21]. Until multi-state devices are available, increased circuit complexity, higher static power requirements and reduced speed performance will continue to plague MVL storage devices in this area.

However, this may not be an entirely fair comparison. As an example, a binary data latch commonly used in VLSI applications is shown in Fig. 7.1. To obtain the same number of logic states that are possessed by a single four-valued data latch requires two such devices. Since each binary storage device consists of eight transistors, a total of 16 active logic elements are required for the four-state equivalent circuit of Fig. 7.2 When compared to the MVL devices of this study, as is done in Table 7.1, two MVL designs can be seen to require the same number of transistors as the binary equivalent circuit. When viewed in this context, circuit complexity, at least for voltage-mode designs, compare favorably with binary implementations.

Another problem encountered in MVL is the static power required to perform input logic level discrimination. For current-mode CMOS designs, the input current must be converted to a voltage signal before the comparator network can perform its function. This is accomplished through the use of a diode-connected transistor and will consume power whenever the input is above logic 0.

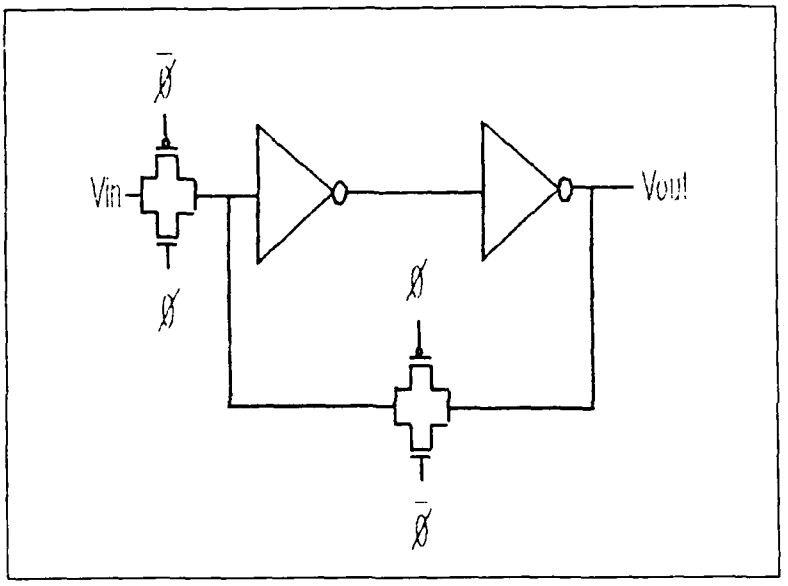


Figure 7.1: Binary Data Latch

TABLE 7.1: MVL VS BINARY - CIRCUIT COMPLEXITY

Number of Active Logic Elements					
Current Mode (Fig. 3.1)	Modified Current Mode (Fig. 4.1)	$V_{dd} = 15$ V Voltage Mode (Fig. 5.5)	$V_{dd} = 5$ V Voltage Mode (Fig. 5.5)	Modified Voltage Mode (Fig. 5.16)	Equivalent Binary Circuit (Fig. 7.1)
27	21	16	16	19	16

For voltage-mode CMOS designs, intermediate logic levels (less than V_{dd}) prevent threshold detector PMOS devices from operating in cutoff. Unlike binary inverters, these devices dissipate power after the transition between logic states has occurred. Although resolving this problem will be difficult in current-mode CMOS, potential solutions exist for voltage-mode designs.

Threshold voltages for both n- and p-type MOS transistors can be adjusted at fabrication through the use of ion implantation [Ref. 22]. (An example four-valued full adder circuit that uses this approach can also be found in this reference). In

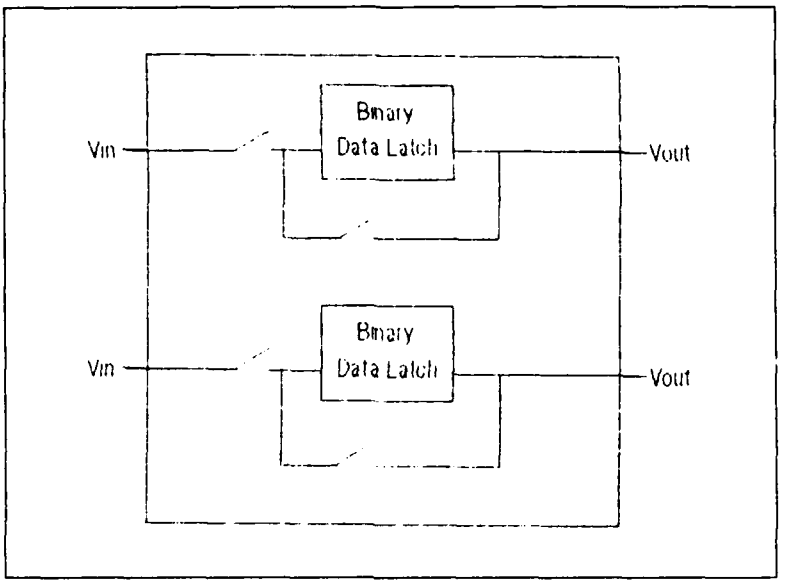


Figure 7.2: Four-State Latch Using Binary Devices

addition, a process called Vertical Injection Punch-Through-based MOS Structure (VIPMOS) can be used to develop an NMOS transistor that has a programmable threshold voltage [Ref. 23]. With threshold voltages capable of being individually set, PMOS devices can be made to operate in cutoff when desired. This stands as a potential solution for reducing static power dissipation in voltage-mode CMOS designs as presented. However, if the programming speed for the VIPMOS transistor can be increased (it is currently only suitable for EEPROM applications) [Ref. 23], the entire voltage-mode latch design could be simplified. Additional research is needed in both of the above areas, as they could significantly improve MVL circuit performance.

As a final problem, MVL devices must either generate, or have access to intermediate logic level power supplies. Since binary devices have only two logic states, V_{dd} and ground suffice for these circuits. However, MVL data latches must either dissipate power to produce these signals or must sacrifice chip area for the routing of their interconnections. This is a fundamental problem for MVL applications in CMOS technology and appears to be unavoidable.

With the combinational circuits of Chapter I providing logic operations at reduced power and in less chip area than binary, perhaps the best comparison between logic types must wait for MVL implementations on a chip-wide basis. The sequential storage devices of this study are the first of many steps needed to achieve that goal.

VIII. CONCLUSIONS

The primary contribution of this thesis is the development of a voltage-mode CMOS data latch suitable for use in sequential MVL applications. To gain an understanding of the requirements this latch needed to possess, an existing current-mode CMOS design was first examined. Comparisons between these devices, as well as for binary implementations have been considered, with the following major conclusions:

— Conclusion 1. Current-mode CMOS designs

Current-mode CMOS designs provide stable intermediate logic states at the expense of static power consumption and circuit complexity. For applications that can withstand these requirements, sequential operations can be performed at higher clock speeds than the VLSI compatible voltage-mode designs of this study.

— Conclusion 2. Voltage-mode CMOS designs

Voltage-mode CMOS designs suitable for VLSI implementation consume less static power than current-mode CMOS designs and can be constructed from the same number of devices as required for two binary data latches, to which it is logically equivalent. Further research is needed in two specific areas: 1) improving intermediate logic level stability; and, 2) investigating the use of individually specified transistor threshold voltages in the design.

— Conclusion 3. Binary devices

Each storage device of this study internally converts a four-valued input signal into three binary control signals. This is a direct result of device technology currently being restricted to binary. Additional research is needed in the area of multi-stable devices. Given this capability, the necessity to convert between logic types can be removed, static power requirements can be reduced and circuit speed increased.

APPENDIX A: PSPICE MODEL PARAMETERS

```
*********************************************
* The following PSPICE model parameters apply*
*   to all latch simulations of this study.  *
*********************************************
*              PMOS Devices                 *
*********************************************
.MODEL TWENTYP PMOS (LEVEL=3
+TPG=-1
+VTO=-.84
+KP=2.15E-5
+GAMMA=.57
+PHI=.7
+TOX=25NM
+NSUB=3.07E16
+NFS=1E10
+VMAX=2.14E05
+ETA=.208
+DELTA=.121
+THETA=5.97E-2
+KAPPA=8.0
+CGSO=1.7E-10
+CGDO=1.7E-10
+CGBO=3.4E-10
+RSH=67
+JS=1E-6
+XJ=1.69E-7
+LD=3.3E-7
+CJ=7.27E-4
+MJ=.41
+CJSW=2.90E-10
+MJSW=.3765
+PB=.91)
*********************************************
*              NMOS Devices                 *
*********************************************
.MODEL TWENTYN NMOS (LEVEL=3
+TPG=1
+VTO=.62
+KP=6.93E-5
+GAMMA=.73
+PHI=.6
+TOX=25NM
+NSUB=2.24E17
+NFS=1E10
```

```
+VMAX=2.09E05
+ETA=.100
+DELTA=.211
+THETA=3.47E-2
+KAPPA=8.83
+CGSO=1.2E-10
+CGDO=1.2E-10
+CGBO=3.4E-10
+RSH=24
+JS=1.5E-5
+XJ=3.5E-7
+ LD=2.27E-7
+CJ=3.36E-4
+MJ=.97
+CJSW=1.34E-10
+MJSW=.65
+PB=.94)
```

APPENDIX B: PSPICE INPUT DATA FILES

```
*****************************************
*          CURRENT-MODE CMOS DESIGN       *
*****************************************
*
*** Thesis figure 3.19  ***
*
*         DEVICES :
*    d  g  s  ss   model
m1    3  3  0  0   TWENTYN  L=3.0u  W=4.5u
m99   3  5  4  0   TWENTYN  L=9.0u  W=9.0u
*
m2    6  4  0  0   TWENTYN  L=3.0u  W=4.5u
m3    6  8  7  1   TWENTYP  L=33.0u W=4.5u
m4   10  6  0  0   TWENTYN  L=3.0u  W=4.5u
m5   10  6  9  1   TWENTYP  L=3.0u  W=4.5u
m6   12 10 13  0   TWENTYN  L=18.0u W=4.5u
m7   12  8 11  1   TWENTYP  L=10.5u W=4.5u
*
m8   14 14 15  0   TWENTYN  L=3.0u  W=4.5u
m98  14 17  4  0   TWENTYN  L=9.0u  W=9.0u
*
m9    8  8 16  1   TWENTYP  L=12.0u W=4.5u
m10   8  8  0  0   TWENTYN  L=49.5u W=4.5u
*
m11  18  4  0  0   TWENTYN  L=3.0u  W=4.5u
m12  18  8 19  1   TWENTYP  L=12.0u W=7.5u
m13  20 18  0  0   TWENTYN  L=3.0u  W=4.5u
m14  20 18 21  1   TWENTYP  L=3.0u  W=4.5u
m15  22 20 13  0   TWENTYN  L=18.0u W=4.5u
m16  22  8 23  1   TWENTYP  L=10.5u W=4.5u
*
m17  24  4  0  0   TWENTYN  L=3.0u  W=4.5u
m18  24  8 25  1   TWENTYP  L=6.0u  W=6.0u
m19  26 24  0  0   TWENTYN  L=3.0u  W=4.5u
m20  26 24 27  1   TWENTYP  L=3.0u  W=4.5u
m21  28 26 13  0   TWENTYN  L=18.0u W=4.5u
m22  28  8 29  1   TWENTYP  L=10.5u W=4.5u
*
m23  30 14  0  0   TWENTYN  L=4.5u  W=6.0u
m24  30 30 31  1   TWENTYP  L=3.0u  W=4.5u
m25  33 30 32  1   TWENTYP  L=3.0u  W=4.5u
*
* M26 IS JUST FOR A PATH TO GROUND ON THE OUTPUT
m26  34 34  0  0   TWENTYN  L=3.0u  W=4.5u
*
```

```
*         PARASITIC CAPACITANCES :
c0    0  0  221.0f
c1    1  0  306.0f
c3    3  0   52.0f
c4    4  0   74.0f
c5    5  0   11.0f
c6    6  0   56.0f
c8    8  0  233.0f
c10 10   0   74.0f
c12 12   0   49.0f
c13 13   0  119.0f
c17 17   0   11.0f
c18 18   0   58.0f
c20 20   0   66.0f
c22 22   0   47.0f
c24 24   0   66.0f
c26 26   0   64.0f
c28 28   0   47.0f
*
*         SOURCES:
iin     1  2 pwl(0ns 0u 500ns 0u 3500ns 30u 6500ns 0u 7500ns 0u)
vdd     1  0 dc 5v
vclk    5  0 pulse(0 5v 0ns 3ns 3ns 200ns 400ns)
vnclk 17   0 pulse(0 5v 190ns 3ns 3ns 220ns 400ns)
*Vpsub 36   0 dc 5v
*Vnsub 35   0 dc 0v
*
*         AMMETERS:
Vampin     2  3
Vampa      1  7
Vampainv   1  9
Vampsum   13 14
Vampsumchk  15  0
Vampia     1 11
Vampref    1 16
*
Vampb      1 19
Vampbinv   1 21
Vampib     1 23
*
Vampc      1 25
Vampcinv   1 27
Vampic     1 29
*
Vampouti   1 31
Vampout    1 32
Vampoutchk 33 34
*
*         TESTS & MISC
```

```
.ic v(13)=0.62
*.tran 1.0ns 4000ns
.tran 1.0ns 7500ns 3500ns
.width out=80
.probe
.options limpts=7001 numdgt=7 defl=5u defw=10u defas=125p defad=125p
+nomod itl1=100 abstol=.1p chgtol=.1p itl5=16000
*
*
*.MODEL TWENTYP PMOS (see Appendix A)
*.MODEL TWENTYN NMOS (see Appendix A)
*
.end
*******************************************
*    MODIFIED CURRENT-MODE CMOS DESIGN    *
*******************************************
*
*** Thesis figure 4.7   ***
*
*        DEVICES :
*   d  g  s  ss   model
m1   3  3  0  0   TWENTYN  L=3.0u  W=4.5u
m99  3  5  4  0   TWENTYN  L=9.0u  W=9.0u
*
m2   6  4  0  0   TWENTYN  L=3.0u  W=4.5u
m3   6  8  7  1   TWENTYP  L=33.0u W=4.5u
****m4  10  6  0  0   TWENTYN  L=3.0u  W=4.5u
****m5  10  6  9  1   TWENTYP  L=3.0u  W=4.5u
m6  12  6 13  1   TWENTYP  L=18.0u W=4.5u
m7  12  8 11  1   TWENTYP  L=10.5u W=4.5u
*
m8  14 14 15  0   TWENTYN  L=3.0u  W=4.5u
m98 14 17  4  0   TWENTYN  L=9.0u  W=9.0u
*
m9   8  8 16  1   TWENTYP  L=12.0u W=4.5u
m10  8  8  0  0   TWENTYN  L=49.5u W=4.5u
*
m11 18  4  0  0   TWENTYN  L=3.0u  W=4.5u
m12 18  8 19  1   TWENTYP  L=12.0u  W=7.5u
****m13 20 18  0  0   TWENTYN  L=3.0u  W=4.5u
****m14 20 18 21  1   TWENTYP  L=3.0u  W=4.5u
m15 22 18 13  1   TWENTYp  L=18.0u W=4.5u
m16 22  8 23  1   TWENTYP  L=10.5u W=4.5u
*
m17 24  4  0  0   TWENTYN  L=3.0u  W=4.5u
m18 24  8 25  1   TWENTYP  L=6.0u  W=6.0u
****m19 26 24  0  0   TWENTYN  L=3.0u  W=4.5u
****m20 26 24 27  1   TWENTYP  L=3.0u  W=4.5u
m21 28 24 13  1   TWENTYp  L=18.0u W=4.5u
m22 28  8 29  1   TWENTYP  L=10.5u W=4.5u
*
```

```
m23 30 14  0  0   TWENTYN  L=4.5u  W=6.0u
m24 30 30 31  1   TWENTYP  L=3.0u  W=4.5u
m25 33 30 32  1   TWENTYP  L=3.0u  W=4.5u
*
* M26 IS JUST FOR A PATH TO GROUND ON THE OUTPUT
m26 34 34  0  0   TWENTYN  L=3.0u  W=4.5u
*
*        PARASITIC CAPACITANCES :
c0   0  0  221.0f
c1   1  0  306.0f
c3   3  0   52.0f
c4   4  0   74.0f
c5   5  0   11.0f
c6   6  0   56.0f
c8   8  0  233.0f
*c10 10  0   74.0f
c12 12  0   49.0f
c13 13  0  119.0f
c17 17  0   11.0f
c18 18  0   58.0f
*c20 20  0   66.0f
c22 22  0   47.0f
c24 24  0   66.0f
*c26 26  0   64.0f
c28 28  0   47.0f
*
*        SOURCES:
iin    1  2 pwl(0ns 0u 100ns 0u 103ns 10u 400ns 10u 403ns 0u 1000ns 0u)
vdd    1  0 dc 5v
vclk   5  0 dc 5v
vnclk 17  0 dc 0v
*
*        AMMETERS:
Vampin    2  3
Vampa     1  7
****Vampainv  1  9
Vampsum  13 14
Vampsumchk  15  0
Vampia    1 11
Vampref   1 16
*
Vampb     1 19
****Vampbinv  1 21
Vampib    1 23
*
Vampc     1 25
****Vampcinv  1 27
Vampic    1 29
*
Vampouti  1 31
Vampout   1 32
```

```
Vampoutchk 33 34
*
*        TESTS & MISC
.ic v(13)=0.62
.tran 1.0ns 1000ns
.width out=80
.probe
.options limpts=7001 numdgt=7 defl=5u defw=10u defas=125p defad=125p
+nomod itl1=100 abstol=.1p chgtol=.1p itl5=16000
*
.MODEL TWENTYP PMOS (see Appendix A)
.MODEL TWENTYP PMOS (see Appendix A)
.end
*****************************************
*    VOLTAGE-MODE CMOS DESIGN (Vdd=15V)   *
*****************************************
*
*** Thesis figure 5.9   ***
*
*        DEVICES :
*   d  g  s  ss   model
m1  3  2  1  1    TWENTYP   L=3.0u W=30.0u
m2  3  2  0  0    TWENTYN   L=21.0u  W=4.5u
m9  10 3  1  1    TWENTYP   L=3.0u  W=4.5u

m3  4  2  1  1    TWENTYP   L=3.0u  W=7.5u
m4  4  2  0  0    TWENTYN   L=4.5u  W=4.5u
m10 8  4  6  1    TWENTYP   L=3.0u  W=4.5u
m11 8  3 10  0    TWENTYN   L=3.0u  W=4.5u

m5  5  2  1  1    TWENTYP   L=10.5u W=4.5u
m6  5  2  0  0    TWENTYN   L=3.0u  W=7.5u
m7  9  5  7  1    TWENTYP   L=3.0u  W=4.5u
m8  9  5  0  0    TWENTYN   L=3.0u  W=4.5u
m12 9  4 10  0    TWENTYN   L=3.0u  W=4.5u

m13 2 12 11  1    TWENTYP   L=3.0u  W=4.5u
m14 2 13 11  0    TWENTYN   L=3.0u  W=4.5u

m15 2 13 10  1    TWENTYP   L=3.0u  W=4.5u
m16 2 12 10  0    TWENTYN   L=3.0u  W=4.5u

*        SOURCES:
Vdd  1  0  dc 15.0v
V2   6  0  dc 10.0v
V1   7  0  dc  5.0v
Vin 11  0  pwl(0ns 0v 1000ns 15v 2000ns 0v)
Vclk  13 0  pulse(0v 15v   0ns 4.0ns 4.0ns 100ns 200ns)
Vnclk 12 0  pulse(15v 0v   0ns 4.0ns 4.0ns 100ns 200ns)
*
*        AMMETERS:
```

```
*
*        TESTS, OPTIONS & MISC
.width out=80
.tran 1.0ns 2000ns
.probe
.options limpts=4001 numdgt=7 defl=5u defw=10u defas=125p defad=125p
+nomod itl1=100 abstol=.1p chgtol=.1p
*
*        MODELS
.MODEL TWENTYP PMOS (see Appendix A)
.MODEL TWENTYP PMOS (see Appendix A)
.end
*****************************************
*    VOLTAGE-MODE CMOS DESIGN (Vdd=5V)    *
*****************************************
*
*** Thesis figure 5.14  ***
*
*        DEVICES :
*   d  g  s  ss   model
m1  3  2  1  1    TWENTYP   L=3.0u W=60.0u
m2  3  2  0  0    TWENTYN   L=60.0u W=4.5u

m3  4  2  1  1    TWENTYP   L=15.0u W=21.0u
m4  4  2  0  0    TWENTYN   L=37.5u W=20.5u

m5  5  2  1  1    TWENTYP   L=30.0u W=4.5u
m6  5  2  0  0    TWENTYN   L=3.0u  W=30.0u

m7  9  5  7  1    TWENTYP   L=3.0u  W=21.0u
m8  9  5  0  0    TWENTYN   L=3.0u  W=21.0u

m9  10 3  1  1    TWENTYP   L=3.0u  W=21.0u
m10 8  4  6  1    TWENTYP   L=3.0u  W=21.0u
m11 8  3  10  0    TWENTYN   L=3.0u W=21.0u
m12 9  4  10  0    TWENTYN   L=3.0u W=18.0u

m13 2 12 11  1    TWENTYP   L=3.0u  W=4.5u
m14 2 13 11  0    TWENTYN   L=3.0u  W=4.5u

m15 2 13 10  1    TWENTYP   L=3.0u  W=4.5u
m16 2 12 10  0    TWENTYN   L=3.0u  W=4.5u

c2  2 0  10f
c10 2 0  10f
*        SOURCES:
Vdd  1  0  dc 5.0v
V2   6  0  dc 3.32v
V1   7  0  dc 2.00v
Vin 11 0  pwl(0ns 0v 1000ns 5v 2000ns 0v)
Vclk  13 0  pulse(0v 5v   0ns 4.0ns 4.0ns 100ns 200ns)
```

```
Vnclk 12 0  pulse(0v 5v 110ns 4.0ns 4.0ns  80ns 200ns)
*
*        AMMETERS:
*
*        TESTS, OPTIONS & MISC
.ic v(2)=0
.width out=80
.tran 1.0ns 2000ns
.probe
.options limpts=4001 numdgt=7 defl=5u defw=10u defas=125p defad=125p
+nomod itl1=100 abstol=.1p chgtol=.1p
*
*        MODELS
.MODEL TWENTYP PMOS (see Appendix A)
.MODEL TWENTYP PMOS (see Appendix A)
.end
**********************************************
* MODIFIED VOLTAGE-MODE CMOS DESIGN (Vdd=5V)*
**********************************************
*
*** Thesis figure 5.19  ***
*
*        DEVICES :
*   d  g  s  ss   model
m1  3  2  1  1    TWENTYP   L=3.0u W=60.0u
m2  3  2  0  0    TWENTYN   L=60.0u W=4.5u

m3  4  2  1  1    TWENTYP   L=15.0u W=21.0u
m4  4  2  0  0    TWENTYN   L=37.5u W=20.5u

m5  5  2  1  1    TWENTYP   L=30.0u W=4.5u
m6  5  2  0  0    TWENTYN   L=3.0u  W=30.0u

m7  9  5  7  1    TWENTYP   L=3.0u  W=21.0u
m8  9  5  0  0    TWENTYN   L=3.0u  W=21.0u

m9  10 3  1  1    TWENTYP   L=3.0u  W=21.0u
m10 8  4  6  1    TWENTYP   L=3.0u  W=21.0u
m11 8  3  10  0    TWENTYN   L=3.0u W=21.0u
m12 9  4  10  0    TWENTYN   L=3.0u W=18.0u

m13 2 12 11  1    TWENTYP   L=3.0u  W=4.5u
m14 2 13 11  0    TWENTYN   L=3.0u  W=4.5u

m15 2 13 10  1    TWENTYP   L=3.0u  W=4.5u
m16 2 12 10  0    TWENTYN   L=3.0u  W=4.5u

m17 1  1  6  0    TWENTYN   L=3.0u  W=30.0u
m18 6  6  7  0    TWENTYN   L=3.0u  W=45.0u
m19 7  7  0  0    TWENTYN   L=22.5u W=4.5u
```

```
c2  2 0  10f
c10 2 0  10f
*        SOURCES:
Vdd  1  0  dc 5.0v
Vin 11 0  pwl(0ns 0v 1000ns 5v 2000ns 0v)
Vclk  13 0  pulse(0v 5v   0ns 4.0ns 4.0ns 100ns 200ns)
Vnclk 12 0  pulse(0v 5v 110ns 4.0ns 4.0ns 80ns 200ns)
*
*        AMMETERS:
*
*        TESTS, OPTIONS & MISC
.ic v(2)=0
.width out=80
.tran 1.0ns 2000ns
.probe
.print tran v(11) v(2) v(10) v(13) v(3) v(4) v(5) v(6) v(7)
.options limpts=4001 numdgt=5 defl=5u defw=10u defas=125p defad=125p
+nomod itl1=100 abstol=.1p chgtol=.1p
*
*        MODELS
.MODEL TWENTYP PMOS (see Appendix A)
.MODEL TWENTYP PMOS (see Appendix A)
.end
```

REFERENCES

1. D. Etiemble and M. Israel, "Comparison of binary and multivalued ICs according to VLSI criteria," *Computer*, Vol. 21, pp. 28-42, April 1988.

2. J. T. Butler, "Guest editor's introduction: multiple-valued logic," *Computer*, Vol. 21, pp. 13-14, April 1988.

3. K. C. Smith, "Multiple-valued logic: a tutorial and appreciation," *Computer*, Vol. 21, pp. 17-27, April 1988.

4. J. T. Butler and H. G. Kerkhoff, "Multiple-valued CCD circuits," *Computer*, Vol. 21, pp. 58-69, April 1988.

5. M. Kameyama, S. Kawahito and T. Higuchi, "A multiplier chip with multiple-valued bi-directional current-mode logic circuits," *Computer*, Vol. 21, pp. 43-56, April 1988.

6. D. Etiemble, "T.S.C. multivalued TTL circuits," *Proceedings of the Tenth International Symposium on Multiple-Valued Logic*, pp. 31-35, May 1980.

7. G. Weinan, "The design of the high speed A/D converter by using multiple-valued logic," *Proceedings of the Nineteenth International Symposium on Multiple-Valued Logic*, pp. 188-194, May 1989.

8. F. Ueno, T. Inoue, K. Sugitani and S. Araki, "A programmable switched capacitor circuit for multivalued-to-binary and binary-to-multivalued conversions," *Proceedings of the Nineteenth International Symposium on Multiple-Valued Logic*, pp. 195-201, May 1989.

9. H. L. Ho and K. C. Smith, "Switched capacitor circuits in the implementation of multiple-valued logic," *Proceedings of the Nineteenth International Symposium on Multiple-Valued Logic*, pp. 202-209, May 1989.

10. K. Hwang and F. A. Briggs, *Computer Architecture and Parallel Processing* pp. 54-55, McGraw-Hill, Inc., 1984.

11. P. Tirumalai and J. T. Butler, "On the realization of multiple-valued logic functions using CCD PLA'S," *Proceedings of the Fourteenth International Symposium on Multiple-Valued Logic*, pp. 33-35, May 1984.

12. W. C. Kabat and A. S. Wojcik, "On the design of 4-valued digital systems," *Proceedings of the Tenth International Symposium on Multiple-Valued Logic*, pp. 153-157, May 1980.

13. K. W. Current, "A CMOS quaternary latch," *Proceedings of the Nineteenth International Symposium on Multiple-Valued Logic*, pp. 54-57, May 1989.

14. X. Xu, S. Li and Z. Cui, "A new current-mode multi-valued storage circuit," *Proceedings of the Nineteenth International Symposium on Multiple-Valued Logic*, pp. 368-375, May 1989.

15. N. Weste and K. Eshraghian, "MOS transistor theory," in *Principles of CMOS VLSI Design*, pp. 43-49, Addison-Wesley, Reading, Massachusetts, 1985.

16. *PSPICE*, Microsim Corporation, 1987.

17. K. W. Current, "A CMOS quartenary latch," preprint.

18. A. Vladimirescu, K. Zhang, A. R. Newtow, D. O. Pederson, A. Sangioivanni-Vincentelli, *Spice User's Guide*, pp. 3-4, University of California, Berkeley, California, 1983.

19. A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 2nd ed., pp. 881, CBS College Publishing, New York, New York, 1987.

20. K. W. Current, "A CMOS quaternary threshold logic full adder circuit with transparent latch," preprint.

21. Z. G. Vranesic and K. C. Smith, "Electornic circuits for multi-valued digital systems," in *Computer Science and Multiple-Valued Logic*, David C. Rine, 2nd ed., pp. 371-373, Elsevier Science Publishers, Amsterdam, The Netherlands, 1984.

22. X. Wu, X. Chen and F. Prosser, "An investigation into quaternary full-adder based on transmission function theory," *Proceedings of the Nineteenth International Symposium on Multiple-Valued Logic*, pp 58-62, May 1989.

23. R. C. M. Wijburg, G. J. Hemink, L. Praamsma and J. Middelhoek, "VIPMOS, a buried local injector for EPROM's," preprint.

INITIAL DISTRIBUTION LIST

		No. of Copies
1.	Defense Technical Information Center Cameron Station Alexandria, Virginia 22304-6145	2
2.	Library, Code 0142 Naval Postgraduate School Monterey, California 93943-5002	2
3.	Chairman, Code 62 Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5002	1
4.	Professor J. T. Butler, Code 62Bu Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5005	6
5.	Professor C. Yang, Code 62Ya Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5005	4
6.	Dr. Hans G. Kerkhoff IC Technology and Electronics Group Department of Electrical Engineering, University of Twente 7500 AE Enschede, The Netherlands	1
7.	Dr. George Abraham, Code 1005 Office of Research and Technology, Applied Physics Naval Research Laboratories 4555 Overlook Ave, N.W Washington, DC 20375	1

8. Dr. Parthasarathy Tirumalai 1
Hewlett-Packard Labs.
1501 Page Mill Rd.
Palo Alto, California 94304

9. LT. David A. York 1
Navy Underwater Systems Center
Newport Laboratory
Newport, Rhode Island 02841